Wideband, > 40dB Adjust Range, Linear in dB VARIABLE GAIN AMPLIFIER

FEATURES

- 150MHz SMALL-SIGNAL BANDWIDTH
- 137MHz, $5V_{PP}$ BANDWIDTH (G = +10V/V)
- 0.1dB GAIN FLATNESS to 28MHz
- 1700V/µs SLEW RATE
- > 40dB GAIN ADJUST RANGE
- HIGH GAIN ACCURACY: 20dB ±0.4dB
- HIGH OUTPUT CURRENT: 160mA

APPLICATIONS

- AGC RECEIVERS with RSSI
- DIFFERENTIAL LINE RECEIVERS
- PULSE AMPLITUDE COMPENSATION
- VARIABLE ATTENUATORS
- DROP-IN UPGRADE TO LMH6502

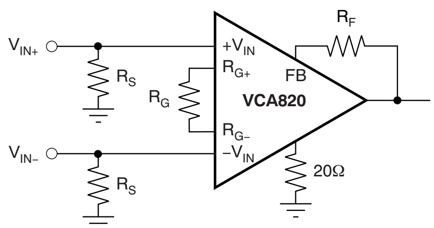


Figure 1. Differential Equalizer

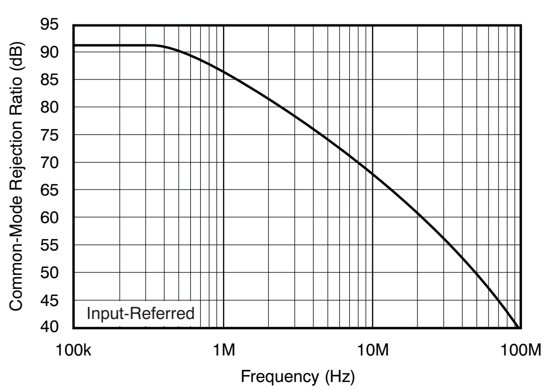


Figure 2. Common-Mode Rejection Ratio

DESCRIPTION

The VCA820 is a dc-coupled, wideband, linear in dB, continuously variable, voltage-controlled gain amplifier. It provides a differential input to single-ended conversion with a high-impedance gain control input used to vary the gain down 40dB from the nominal maximum gain set by the gain resistor (R_G) and feedback resistor (R_F).

The VCA820 internal architecture consists of two input buffers and an output current feedback amplifier stage integrated with a multiplier core to provide a complete variable gain amplifier (VGA) system that does not require external buffering. The maximum gain is set externally with two resistors, providing flexibility in designs. The maximum gain is intended to be set between +2V/V and +100V/V. Operating from ±5V supplies, the gain control voltage for the VCA820 adjusts the gain linearly in dB as the control voltage varies from 0V to +2V. For example, set for a maximum gain of +10V/V, the VCA820 provides 20dB, at +2V input, to –20dB at 0V input of gain control range. The VCA820 offers excellent gain linearity. For a 20dB maximum gain, and a gain-control input voltage varying between 1V and 2V, the gain does not deviate by more than ±0.4dB (maximum at +25°C).

VCA820 RELATED PRODUCTS

SINGLES	DUALS	GAIN ADJUST RANGE (dB)	INPUT NOISE (nV/√Hz)	SIGNAL BANDWIDTH (MHz)
VCA810	—	80	2.4	35
—	VCA2612	45	1.25	80
—	VCA2613	45	1	80
—	VCA2615	52	0.8	50
—	VCA2617	48	4.1	50
VCA820	—	40	8.2	150
VCA821	—	40	7.0	420
VCA822	—	40	8.2	150
VCA824	—	40	7.0	420

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VCA820	SO-14	D	–40°C to +85°C	VCA820ID	VCA820ID	Rail, 50
					VCA820IDR	Tape and Reel, 2500
VCA820	MSOP-10	DGS	–40°C to +85°C	BOQ	VCA820IDGST	Tape and Reel, 250
					VCA820IDGSR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

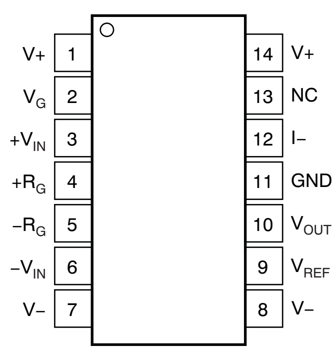
Over operating free-air temperature range, unless otherwise noted.

		VCA820	UNIT
Power supply		±6.3	V
Internal power dissipation		See Thermal Characteristics	
Input voltage range		$\pm V_S$	V
Storage temperature range		–65 to +125	°C
Lead temperature (soldering, 10s)		+260	°C
Junction temperature (T_J)		+150	°C
Junction temperature (T_J), maximum continuous operation		+140	C
ESD rating:	Human body model (HBM)	2000	V
	Charge device model (CDM)	500	V
	Machine model	200	V

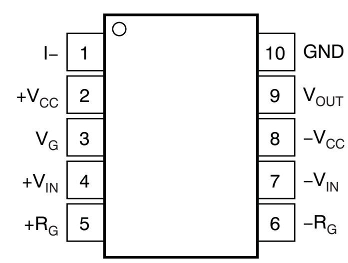
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

PIN CONFIGURATIONS

SO-14
(Top View)



MSOP-10
(Top View)



ELECTRICAL CHARACTERISTICS: V_S = ±5V

At A_{VMAX} = 20dB, R_F = 1kΩ, R_G = 200Ω, and R_L = 100Ω, unless otherwise noted.

		VCA820						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C(2)	0°C to +70°C(3)	–40°C to +85°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
AC PERFORMANCE								
Small-signal bandwidth (SO-14 package)	A_{VMAX} = 6dB, V_O = $1V_{PP}$, V_G = +2V	168				MHz	typ	C
	A_{VMAX} = 20dB, V_O = $1V_{PP}$, V_G = +2V	150				MHz	typ	C
	A_{VMAX} = 40dB, V_O = $1V_{PP}$, V_G = +2V	118				MHz	typ	C
Large-signal bandwidth	A_{VMAX} = 20dB, V_O = $5V_{PP}$, V_G = +2V	137				MHz	typ	C
Gain control bandwidth	V_G = $1V_{DC}$ + $10mV_{PP}$	200	170	170	165	MHz	min	B
Bandwidth for 0.1dB flatness	A_{VMAX} = 20dB, V_O = $1V_{PP}$, V_G = +2V	28				MHz	typ	C
Slew rate	A_{VMAX} = 20dB, V_O = 5V step, V_G = +2V	1700	1500	1500	1450	V/µs	min	B
Rise-and-fall time	A_{VMAX} = 20dB, V_O = 5V step, V_G = +2V	2.5	3.1	3.2	3.2	ns	max	B
Settling time to 0.01%	A_{VMAX} = 20dB, V_O = 5V step, V_G = +2V	11				ns	typ	C
Harmonic distortion								
2nd-harmonic	V_O = $2V_{PP}$, f = 20MHz	–62	–60	–60	–60	dBc	min	B
3rd-harmonic	V_O = $2V_{PP}$, f = 20MHz	–68	–66	–66	–66	dBc	min	B
Input voltage noise	f > 100kHz	8.2				nV/√Hz	typ	C
Input current noise	f > 100kHz	2.6				pA/√Hz	typ	C
GAIN CONTROL								
Absolute gain error	A_{VMAX} = 20dB, V_G = 2V	±0.1	**±0.4**	±0.5	±0.6	dB	max	A
V_{CTRL0}		0.85				V	typ	C
V_{SLOPE}		0.09				V	typ	C
Absolute gain error	A_{VMAX} = 20dB, V_G = 1V, (G = 18.06dB)	±0.3	**±0.4**	±0.5	±0.6	dB	max	A
Gain at V_G = 0.2V	Relative to maximum gain	–26	**–24**	–24	–23	dB	max	A
Gain control bias current		10	**16**	16.6	16.7	µA	max	A
Average gain control bias current drift				±12	±12	nA/°C	max	B
Gain control input impedance		70 || 1				kΩ || pF	typ	C
DC PERFORMANCE								
Input offset voltage	A_{VMAX} = 20dB, V_{CM} = 0V, V_G = 1V	±4	**±17**	±17.8	±19	mV	max	A
Average input offset voltage drift	A_{VMAX} = 20dB, V_{CM} = 0V, V_G = 1V			30	30	µV/°C	max	B
Input bias current	A_{VMAX} = 20dB, V_{CM} = 0V, V_G = 1V	19	**25**	29	31	µA	max	A
Average input bias current drift	A_{VMAX} = 20dB, V_{CM} = 0V, V_G = 1V			90	90	nA/°C	max	B
Input offset current	A_{VMAX} = 20dB, V_{CM} = 0V, V_G = 1V	±0.5	**±2.5**	±3.2	±3.5	µA	max	A
Average input offset current drift	A_{VMAX} = 20dB, V_{CM} = 0V, V_G = 1V			±16	±16	nA/°C	max	B
Maximum current through gain resistance		±2.6	±2.55	±2.55	±2.5	mA	max	B
INPUT								
Most positive common-mode input voltage	R_L = 100Ω	+1.6	**+1.6**	+1.6	+1.6	V	min	A
Most negative common-mode input voltage	R_L = 100Ω	–2.1	**–2.1**	–2.1	–2.1	V	max	A
Common-mode rejection ratio	V_{CM} = ±0.5V	80	**65**	60	60	dB	min	A
Input impedance								
Differential		0.5 || 1				MΩ || pF	typ	C
Common-mode		0.5 || 2				MΩ || pF	typ	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

At A_{VMAX} = 20dB, R_F = 1kΩ, R_G = 200Ω, and R_L = 100Ω, unless otherwise noted.

		VCA820						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C(2)	0°C to +70°C(3)	–40°C to +85°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
OUTPUT								
Output voltage swing	R_L = 1kΩ	±4.0	**±3.8**	±3.75	±3.7	V	min	A
	R_L = 100Ω	±3.9	**±3.7**	±3.6	±3.5	V	min	A
Output current	V_O = 0V, R_L = 5Ω	±160	**±140**	±130	±130	mA	min	A
Output impedance	A_{VMAX} = 20dB, f > 100kHz, V_G = +2V	0.01				Ω	typ	C
POWER SUPPLY								
Specified operating voltage		±5				V	typ	C
Minimum operating voltage		±3.5				V	typ	C
Maximum operating voltage			**±6**	±6	±6	V	max	A
Maximum quiescent current	V_G = 1V	34	**35**	35.5	36	mA	max	A
Minimum quiescent current	V_G = 1V	34	**32.5**	32	31.5	mA	max	A
Power-supply rejection ratio (–PSRR)		–68	**–61**	–59	–58	dB	min	A
THERMAL CHARACTERISTICS								
Specified operating range, D package		–40 to +85				°C	typ	C
Thermal resistance θ_{JA}	Junction-to-ambient							
DGS MSOP-10		130				°C/W	typ	C
D SO-14		80				°C/W	typ	C

TYPICAL CHARACTERISTICS: V_S = ±5V, DC Parameters

At T_A = +25°C, R_L = 100Ω, V_G = +1V, and V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, unless otherwise noted.

MAXIMUM DIFFERENTIAL INPUT VOLTAGE vs GAIN RESISTOR

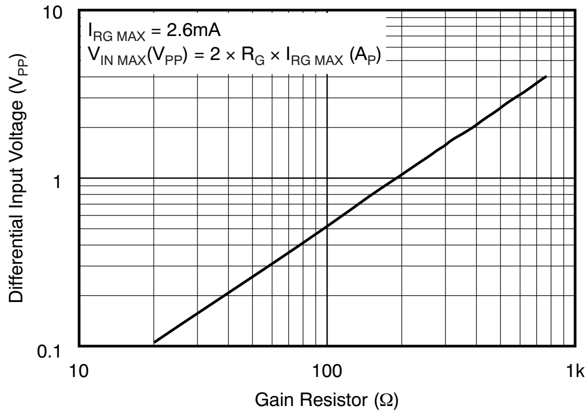


Figure 3.

MAXIMUM GAIN ADJUST RANGE vs FEEDBACK RESISTOR

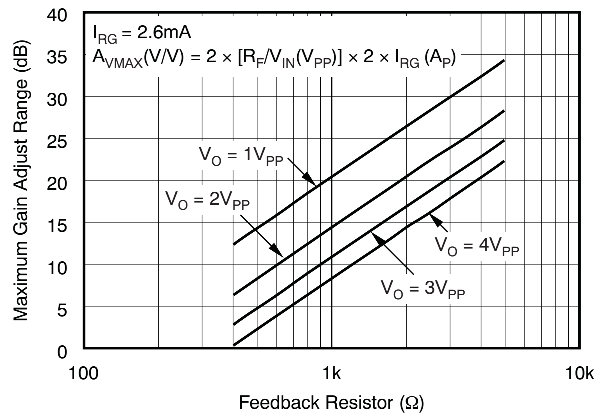


Figure 4.

MAXIMUM GAIN ADJUST RANGE vs PEAK-TO-PEAK OUTPUT VOLTAGE

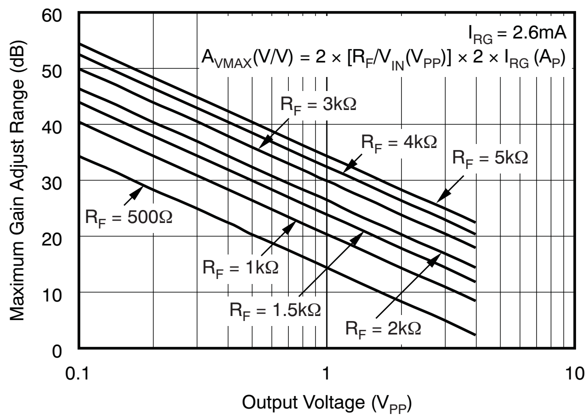


Figure 5.

GAIN ERROR BAND vs GAIN CONTROL VOLTAGE

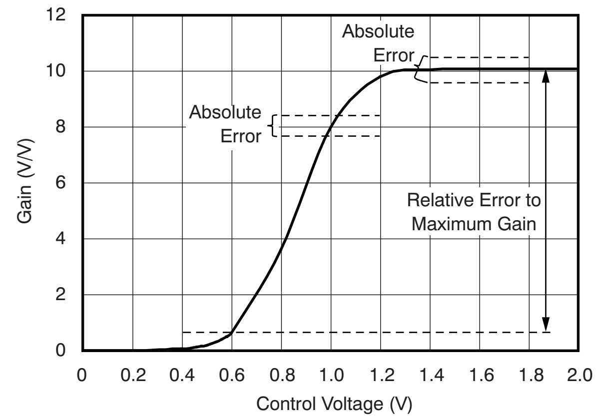


Figure 6.

NOMINAL GAIN vs CALCULATED GAIN

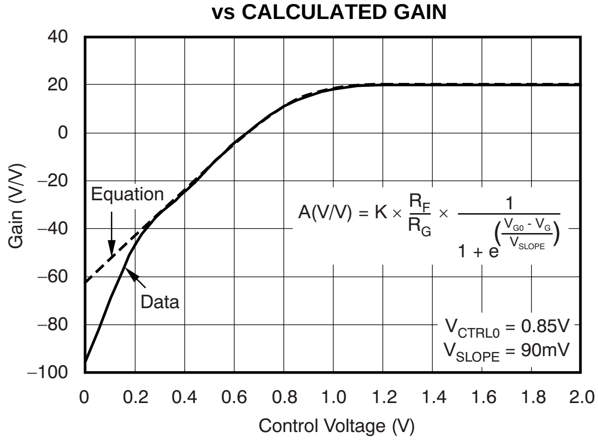


Figure 7.

RECOMMENDED R_F and R_G vs A_{VMAX}

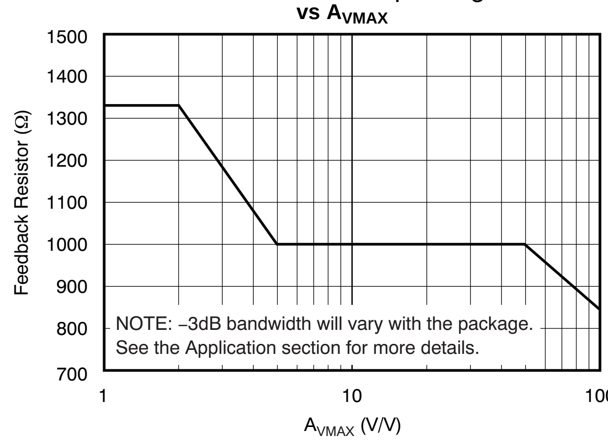


Figure 8.

TYPICAL CHARACTERISTICS: V_S = ±5V, DC and Power-Supply Parameters

At T_A = +25°C, R_L = 100Ω, V_G = +1V, and V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, unless otherwise noted.

SUPPLY CURRENT vs CONTROL VOLTAGE (A_{VMAX} = 6dB)

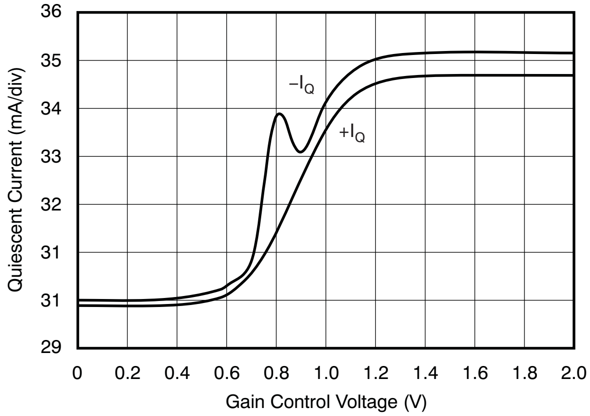


Figure 9.

SUPPLY CURRENT vs CONTROL VOLTAGE (A_{VMAX} = 20dB)

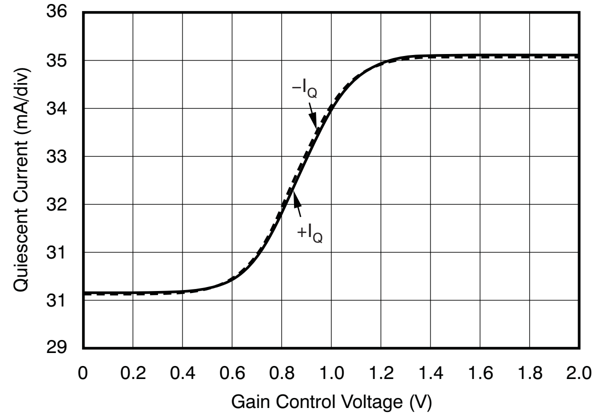


Figure 10.

SUPPLY CURRENT vs CONTROL VOLTAGE (A_{VMAX} = 40dB)

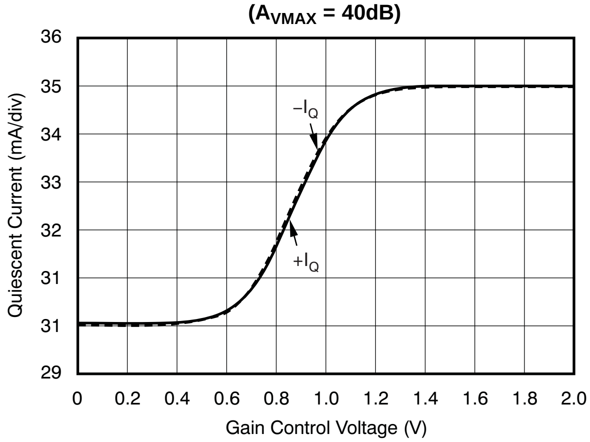


Figure 11.

TYPICAL DC DRIFT vs TEMPERATURE

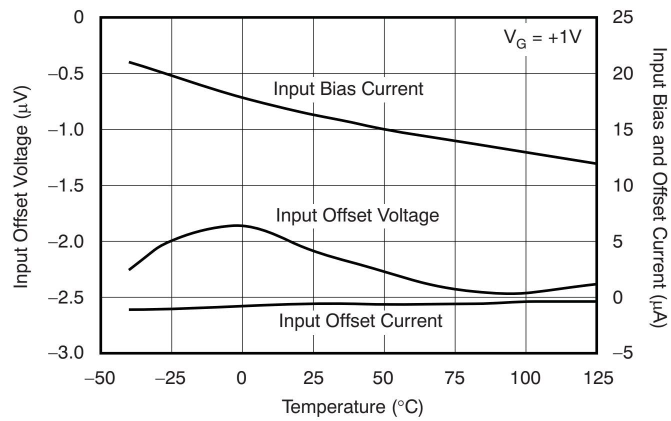


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = 6dB

At T_A = +25°C, R_L = 100Ω, R_F = 1.33kΩ, R_G = 1.33kΩ, V_G = +2V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

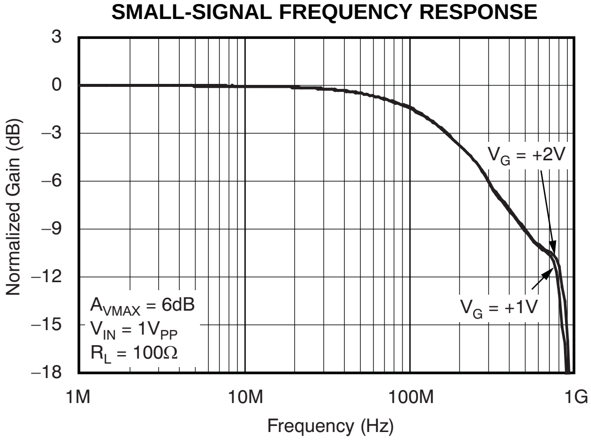


Figure 13.

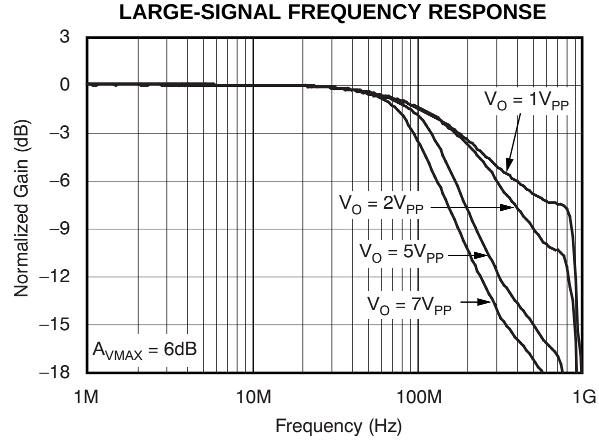


Figure 14.

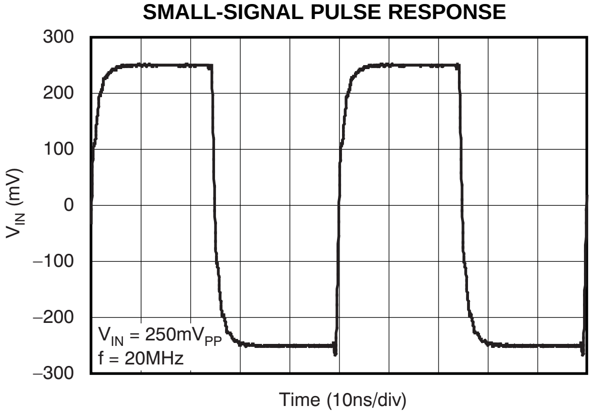


Figure 15.

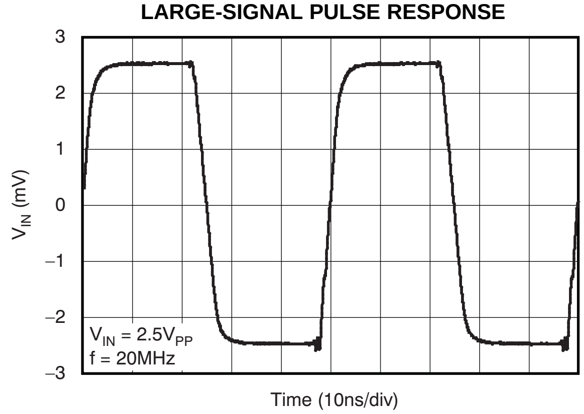


Figure 16.

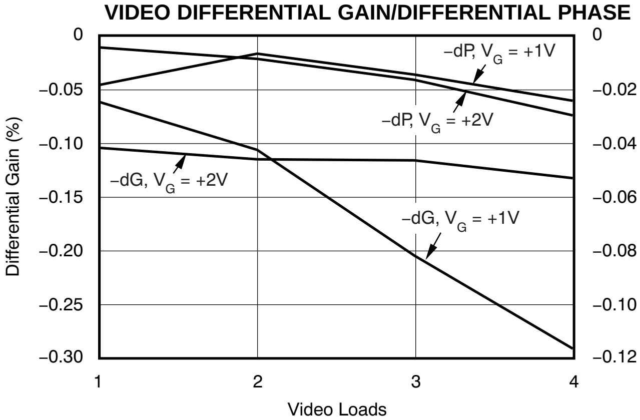


Figure 17.

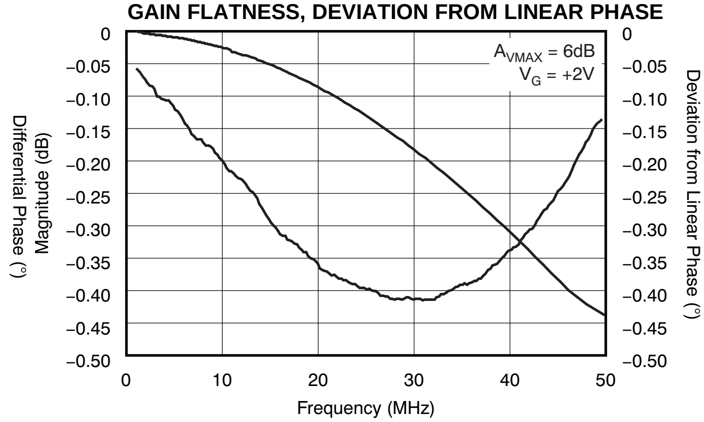


Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = 6dB (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 1.33kΩ, R_G = 1.33kΩ, V_G = +2V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

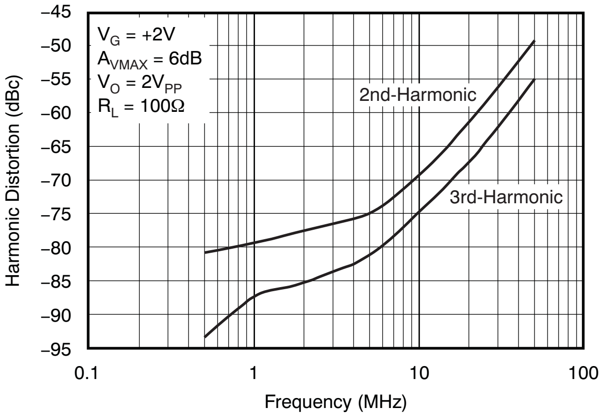


Figure 19.

HARMONIC DISTORTION vs LOAD RESISTANCE

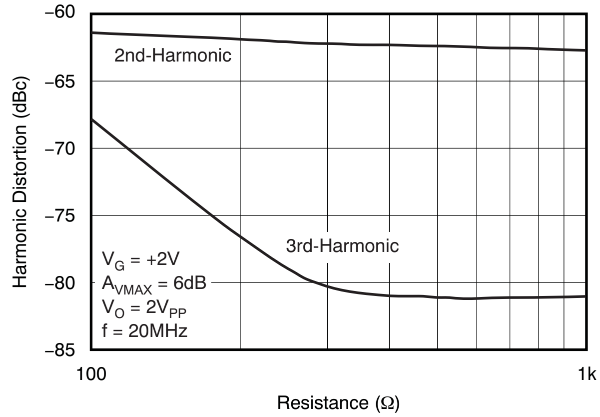


Figure 20.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

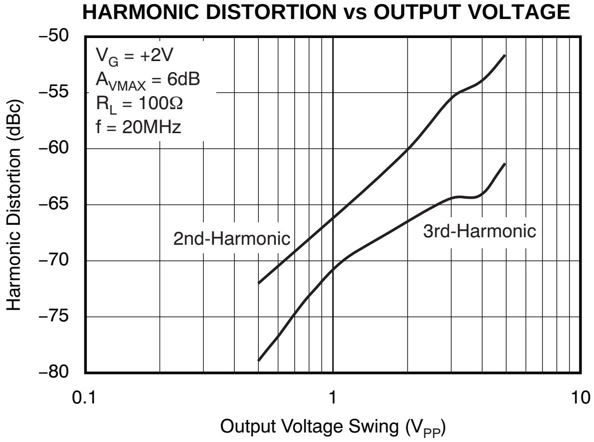


Figure 21.

20MHz HARMONIC DISTORTION vs GAIN CONTROL VOLTAGE

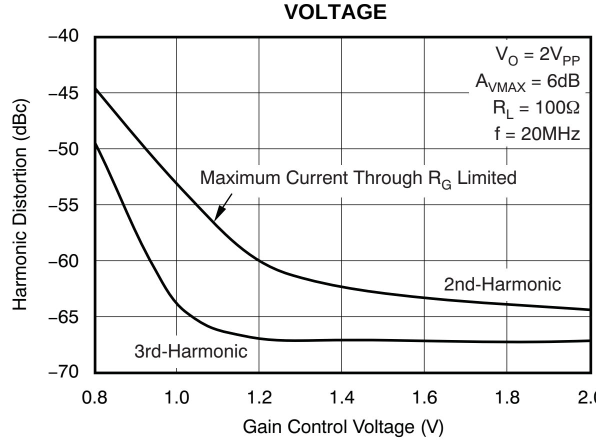


Figure 22.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

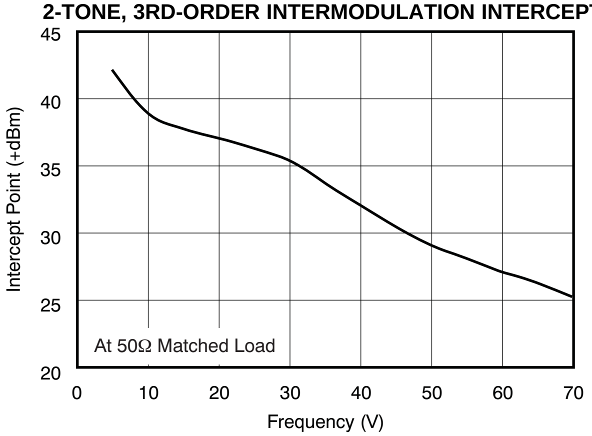


Figure 23.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT vs GAIN CONTROL VOLTAGE

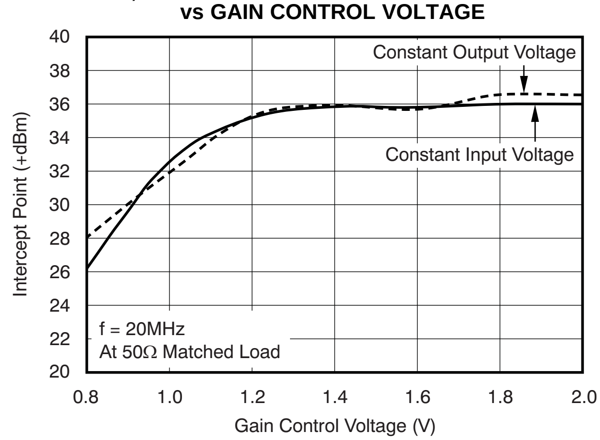


Figure 24.

TYPICAL CHARACTERISTICS: $V_S = \pm 5V$, $A_{VMAX} = 6dB$ (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 1.33kΩ, R_G = 1.33kΩ, V_G = +2V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

GAIN vs GAIN CONTROL VOLTAGE

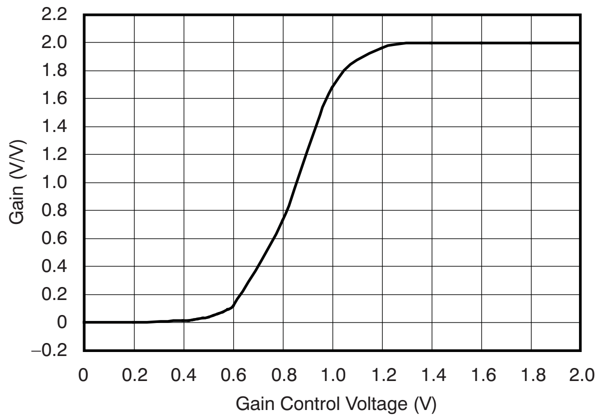


Figure 25.

GAIN CONTROL FREQUENCY

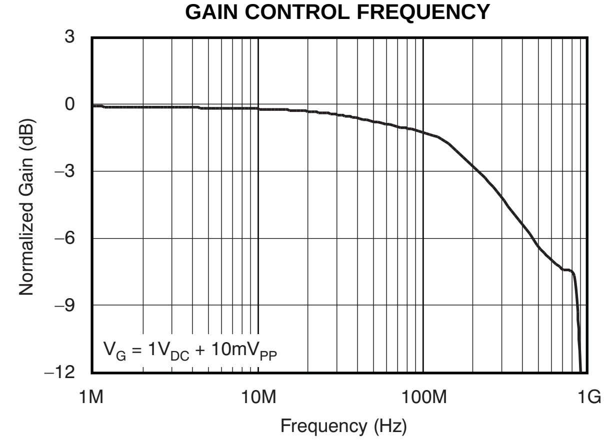


Figure 26.

GAIN CONTROL PULSE RESPONSE

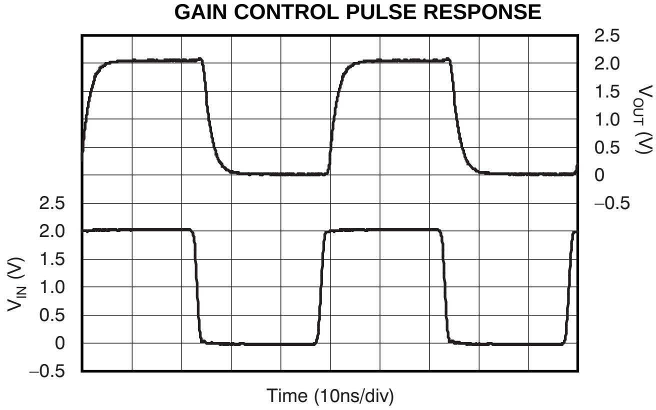


Figure 27.

FULLY-ATTENUATED RESPONSE

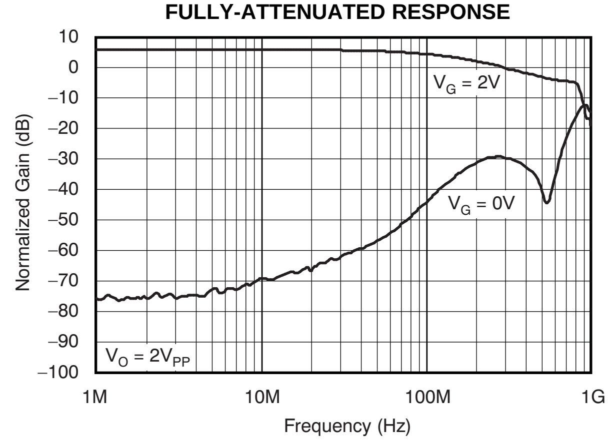


Figure 28.

GROUP DELAY vs GAIN CONTROL VOLTAGE

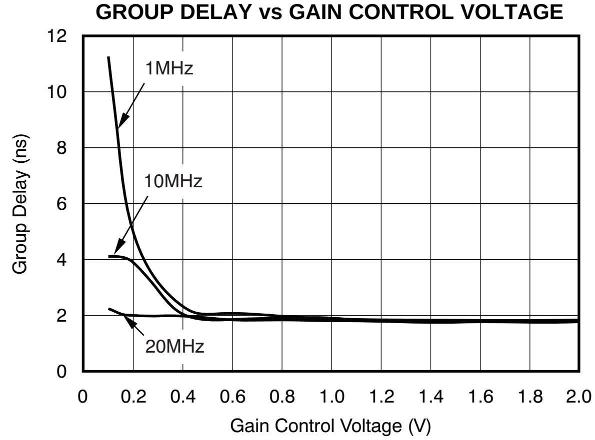


Figure 29.

GROUP DELAY vs FREQUENCY

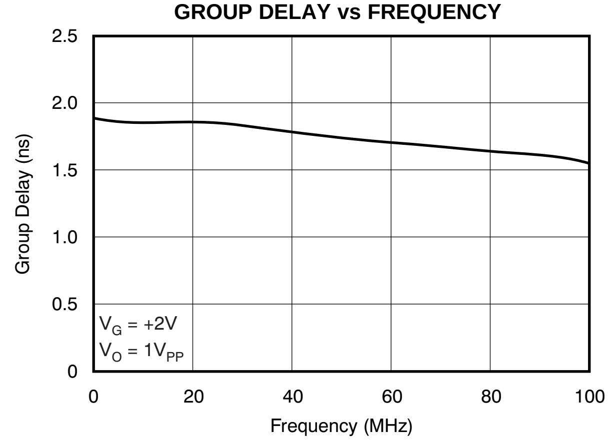


Figure 30.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = 6dB (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 1.33kΩ, R_G = 1.33kΩ, V_G = +2V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

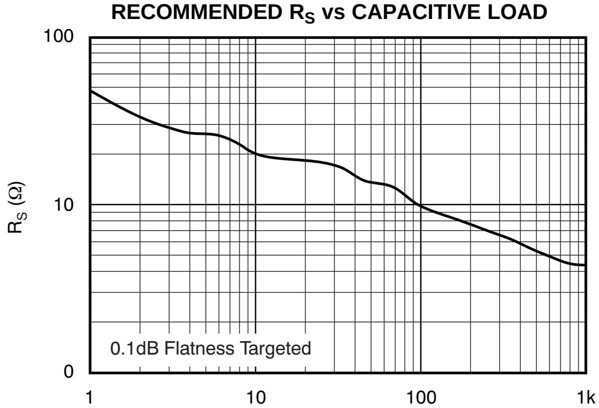


Figure 31.

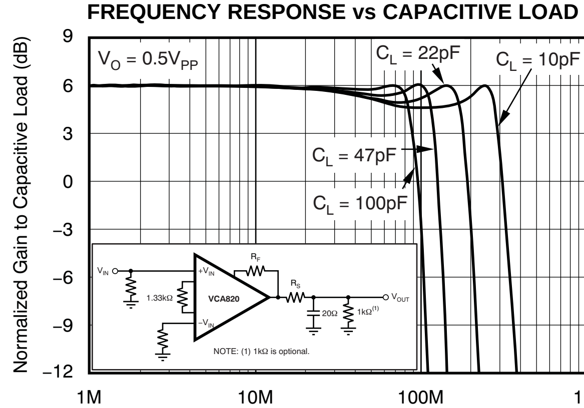


Figure 32.

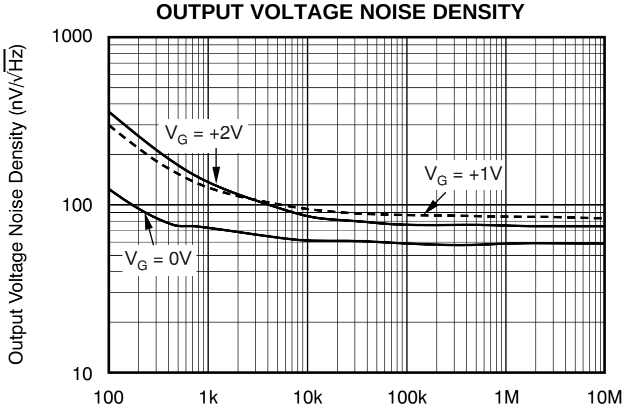


Figure 33.

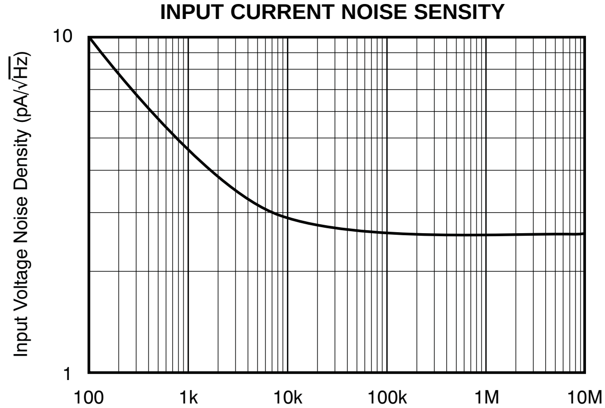


Figure 34.

TYPICAL CHARACTERISTICS: $V_S = \pm 5V$, $A_{VMAX} = 20dB$

At $T_A = +25°C$, $R_L = 100\Omega$, $R_F = 1k\Omega$, $R_G = 200\Omega$, $V_G = +2V$, and V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

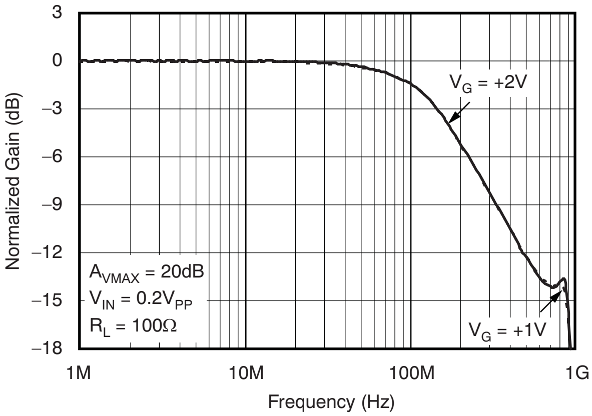


Figure 35.

LARGE-SIGNAL FREQUENCY RESPONSE

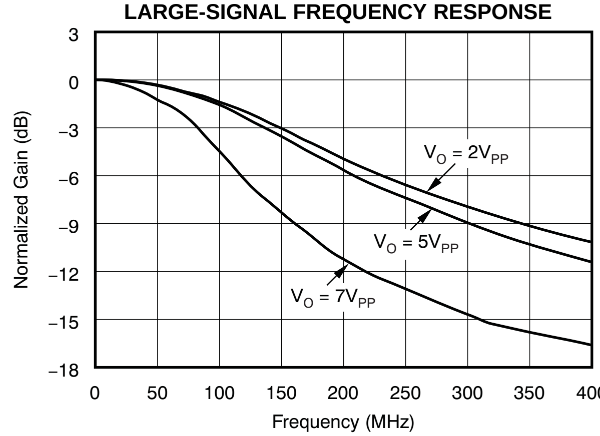


Figure 36.

SMALL-SIGNAL PULSE RESPONSE

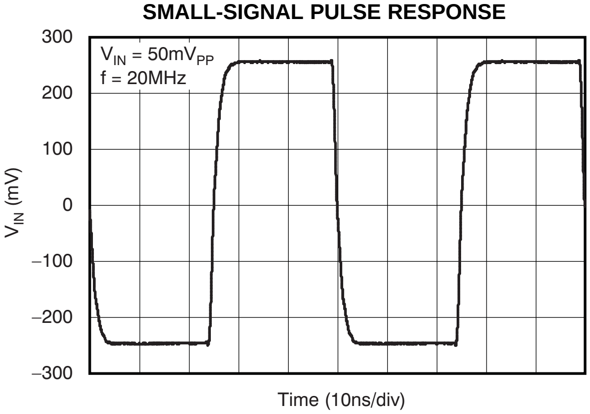


Figure 37.

LARGE-SIGNAL PULSE RESPONSE

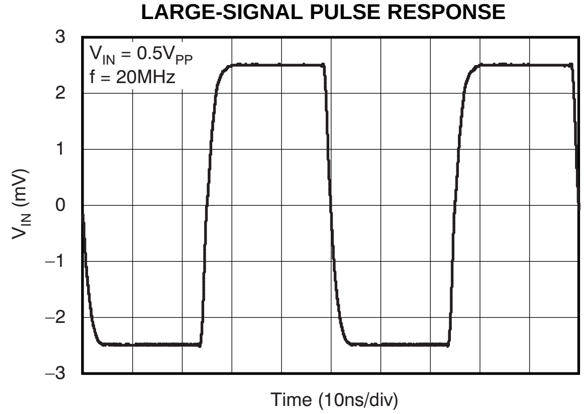


Figure 38.

GAIN FLATNESS, DEVIATION FROM LINEAR PHASE

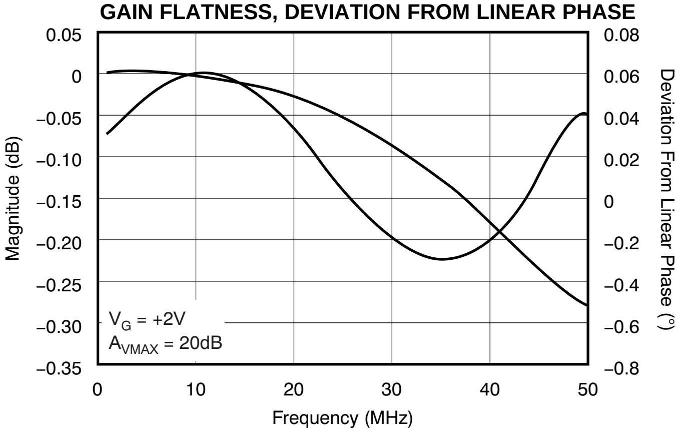


Figure 39.

OUTPUT VOLTAGE NOISE DENSITY

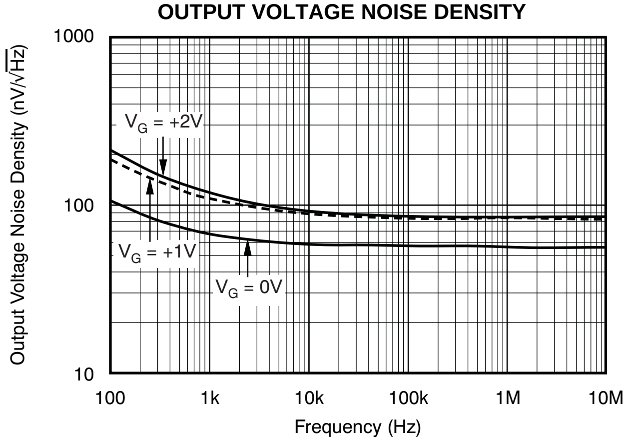


Figure 40.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = 20dB (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 1kΩ, R_G = 200Ω, V_G = +2V, and V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, unless otherwise noted.

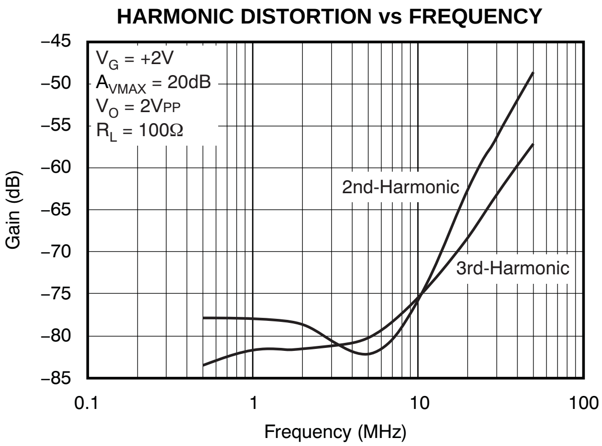


Figure 41.

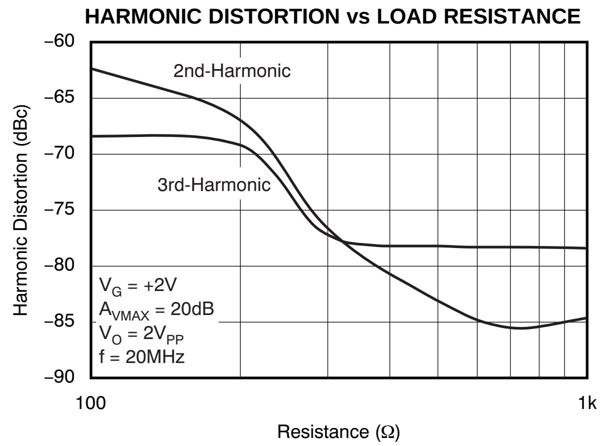


Figure 42.

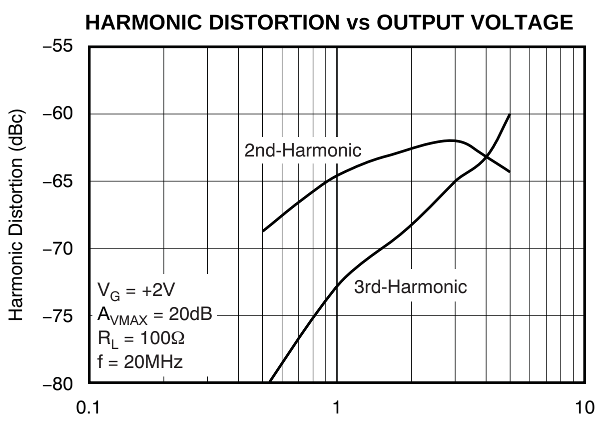


Figure 43.

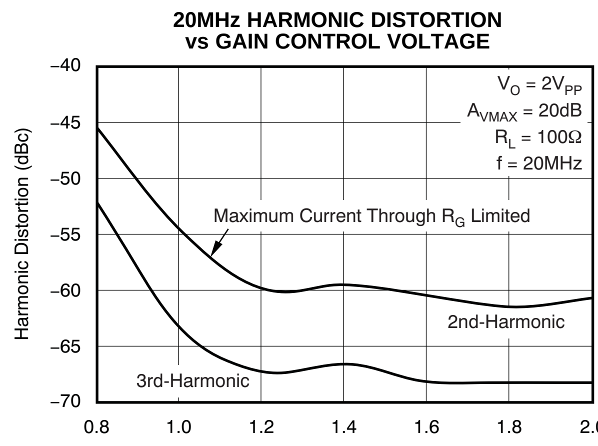


Figure 44.

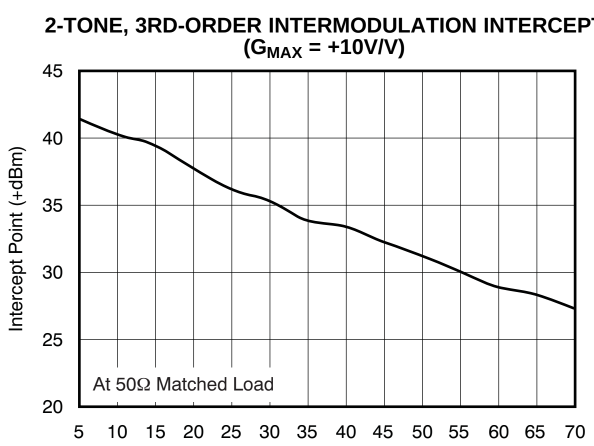


Figure 45.

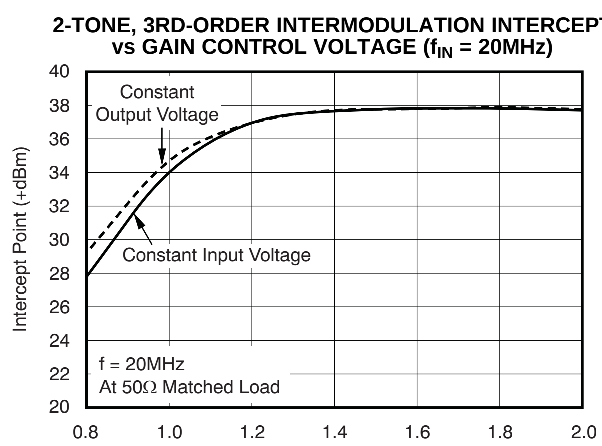


Figure 46.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = 20dB (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 1kΩ, R_G = 200Ω, V_G = +2V, and V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, unless otherwise noted.

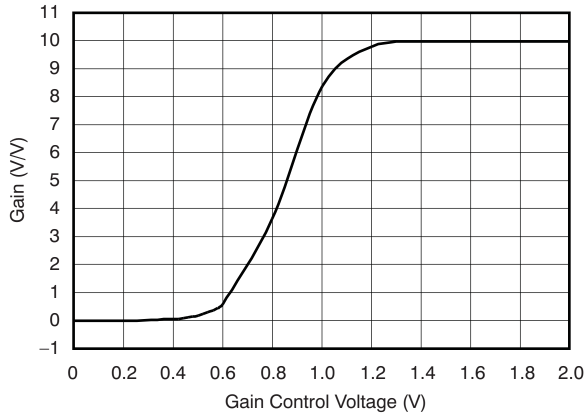


Figure 47.

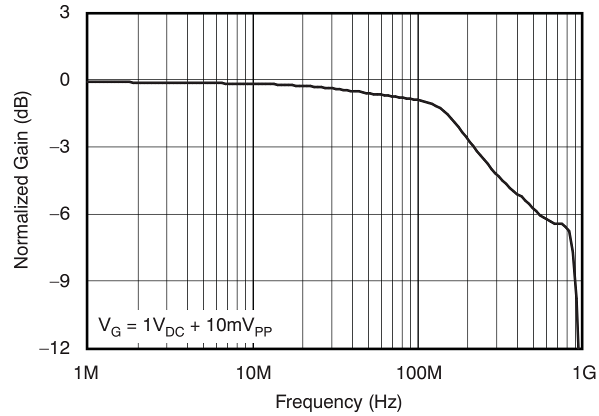


Figure 48.

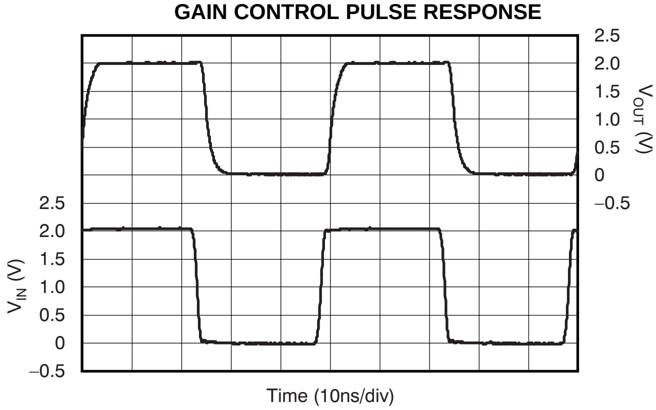


Figure 49.

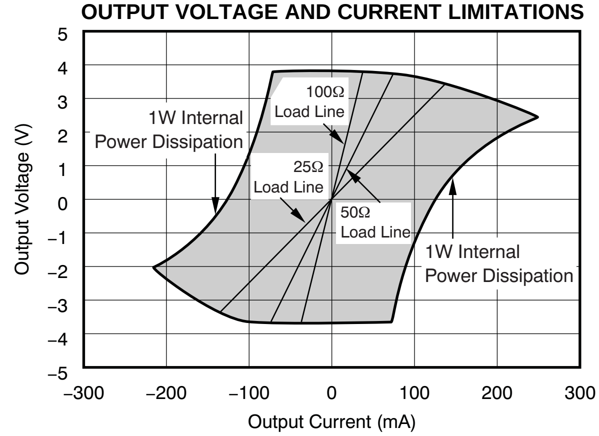


Figure 50.

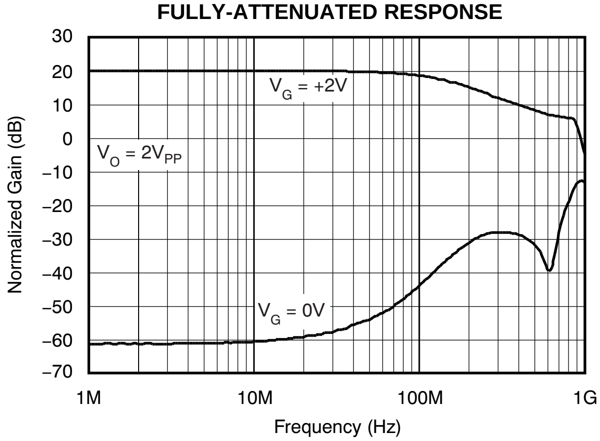


Figure 51.

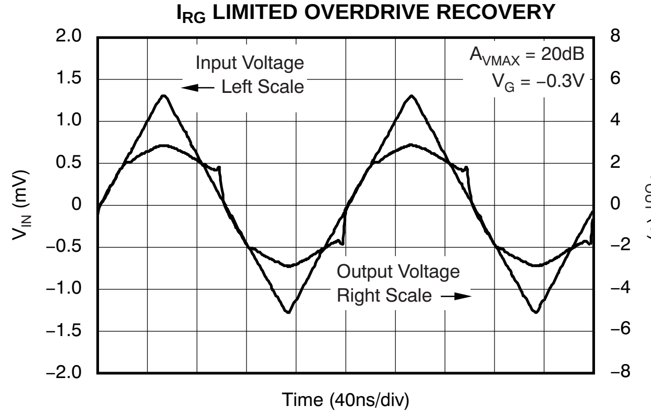


Figure 52.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = 20dB (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 1kΩ, R_G = 200Ω, V_G = +2V, and V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, unless otherwise noted.

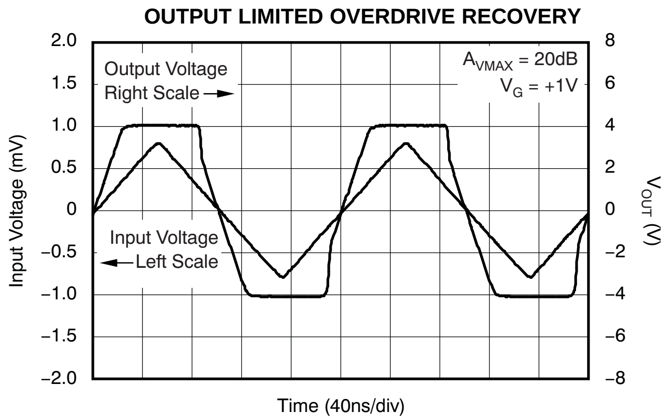


Figure 53.

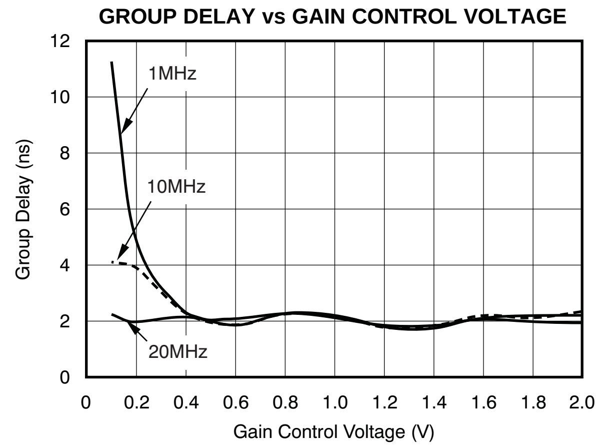


Figure 54.

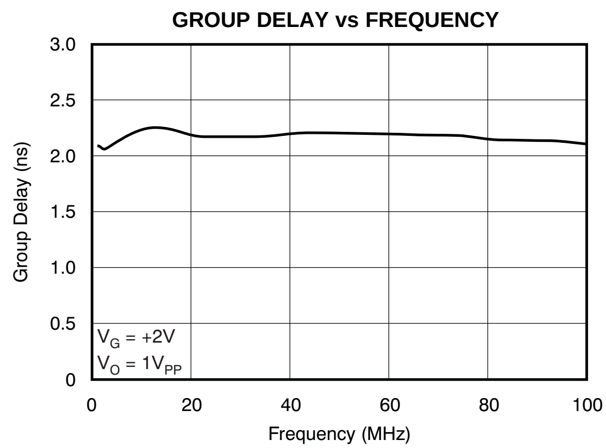


Figure 55.

TYPICAL CHARACTERISTICS: $V_S = \pm 5V$, $A_{VMAX} = 40dB$

At $T_A = +25°C$, $R_L = 100\Omega$, $R_F = 845\Omega$, $R_G = 16.9\Omega$, $V_G = +2V$, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

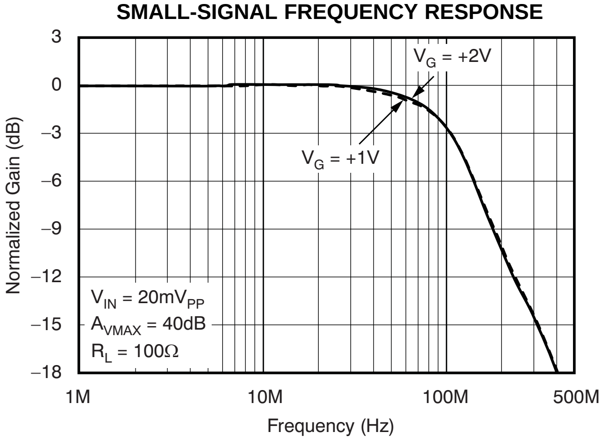


Figure 56.

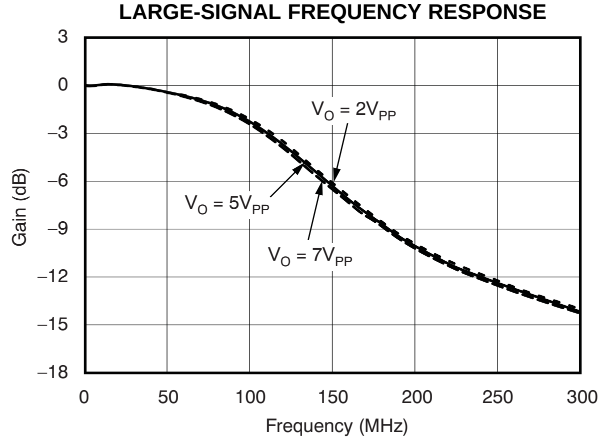


Figure 57.

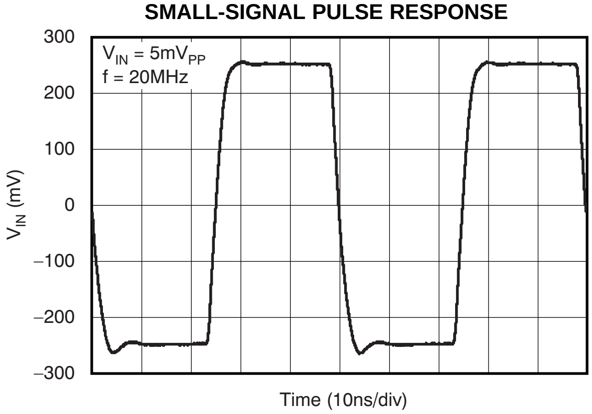


Figure 58.

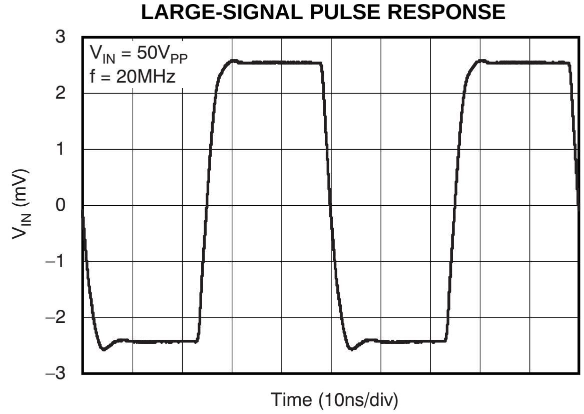


Figure 59.

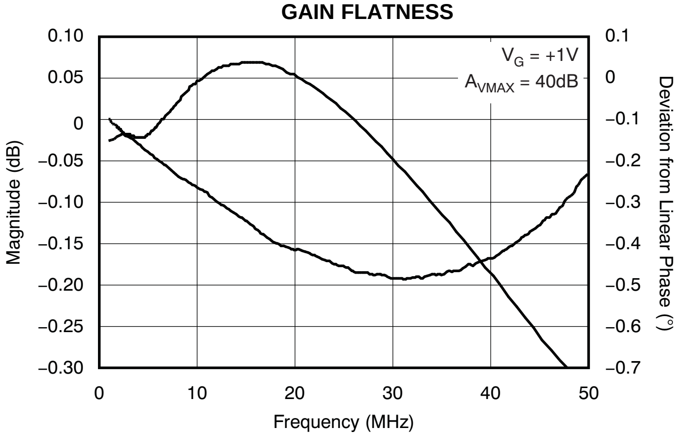


Figure 60.

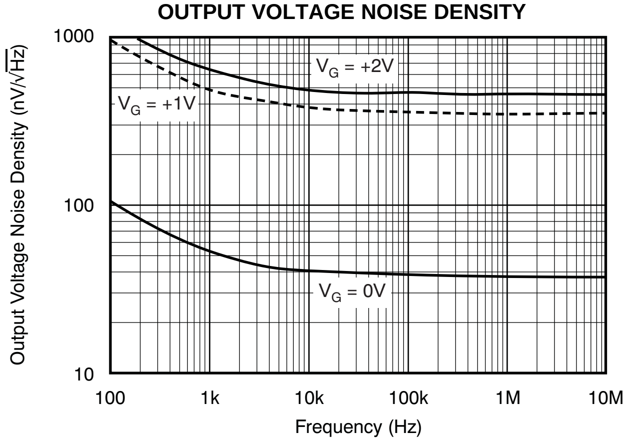


Figure 61.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = 40dB (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 845Ω, R_G = 16.9Ω, V_G = +2V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

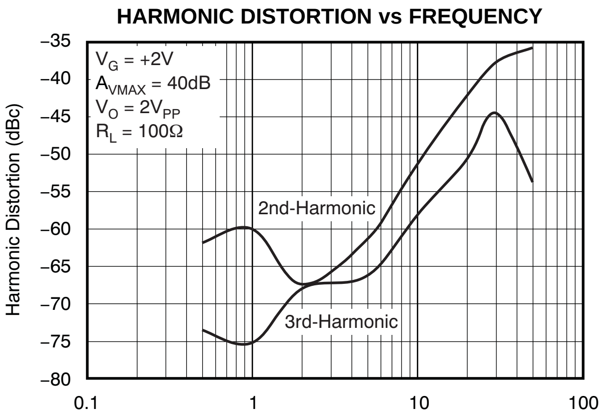


Figure 62.

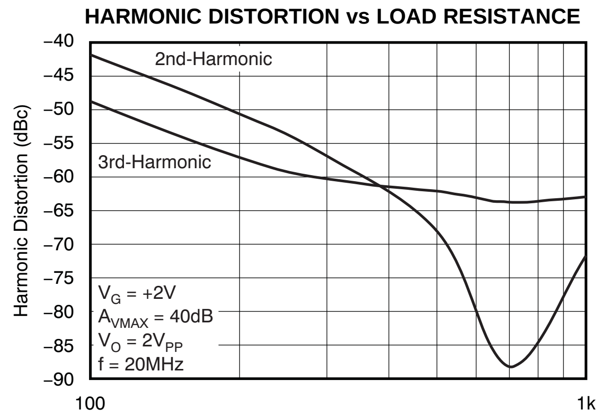


Figure 63.

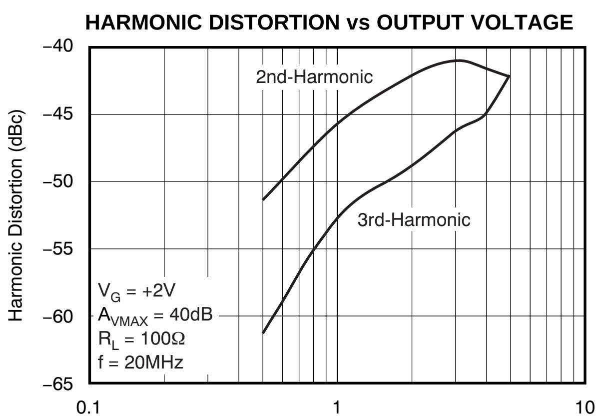


Figure 64.

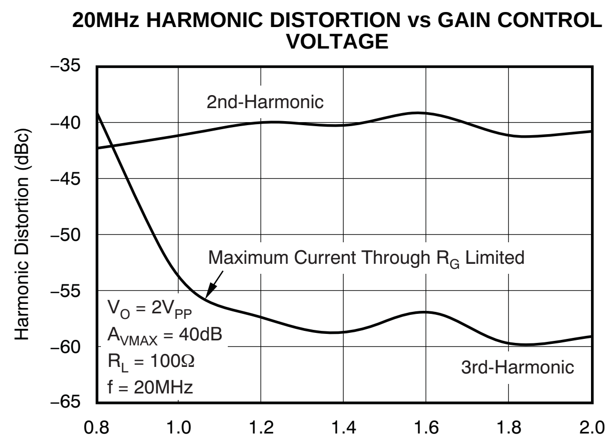


Figure 65.

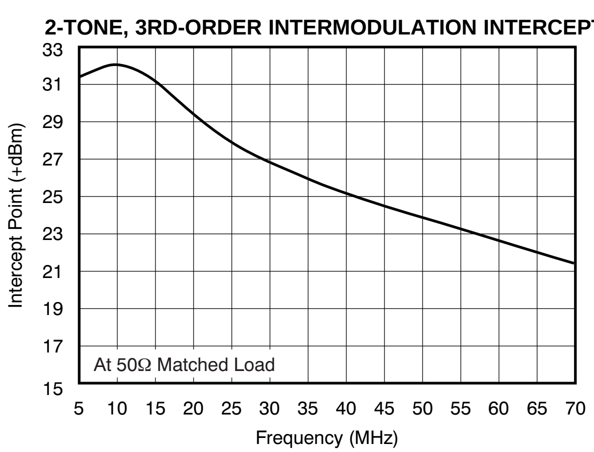


Figure 66.

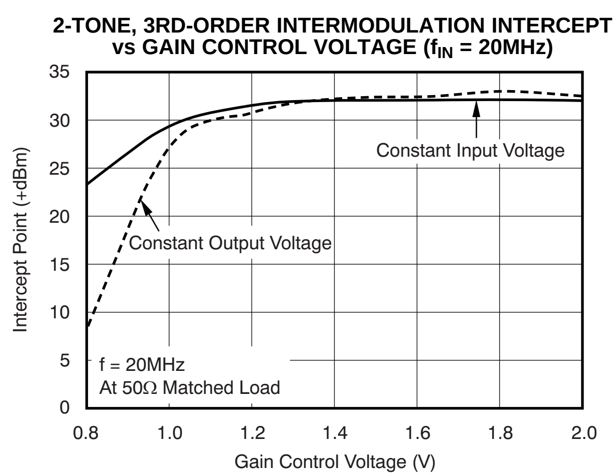


Figure 67.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = 40dB (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 845Ω, R_G = 16.9Ω, V_G = +2V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

GAIN vs GAIN CONTROL VOLTAGE

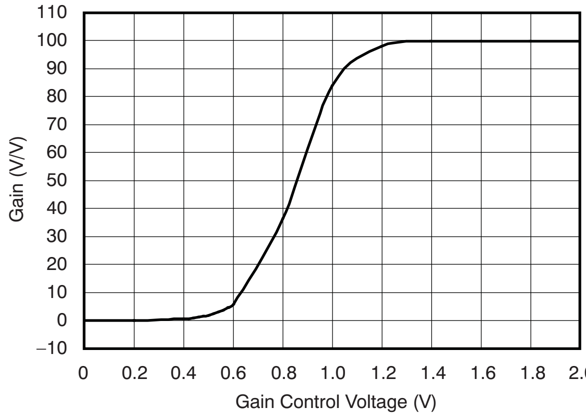


Figure 68.

GAIN CONTROL FREQUENCY

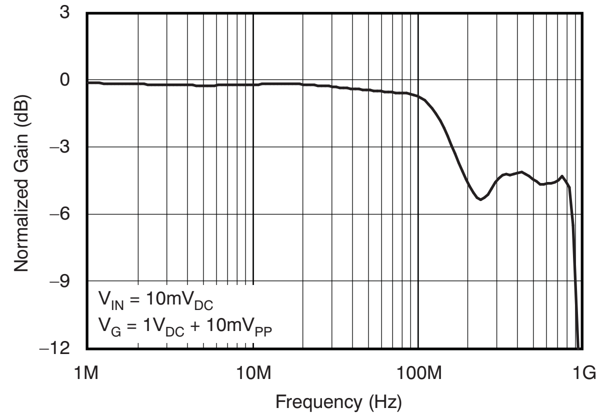


Figure 69.

GAIN CONTROL PULSE RESPONSE

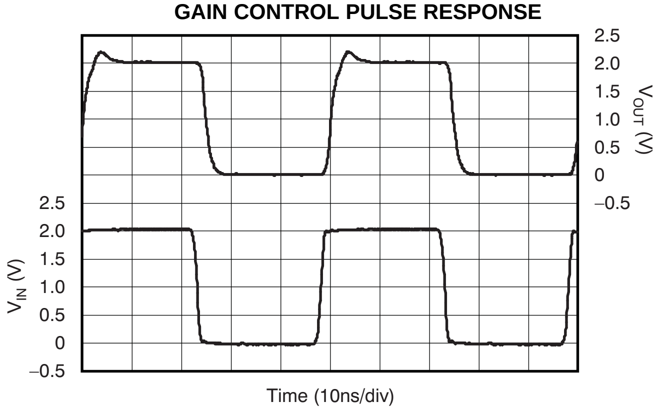


Figure 70.

FULLY-ATTENUATED RESPONSE

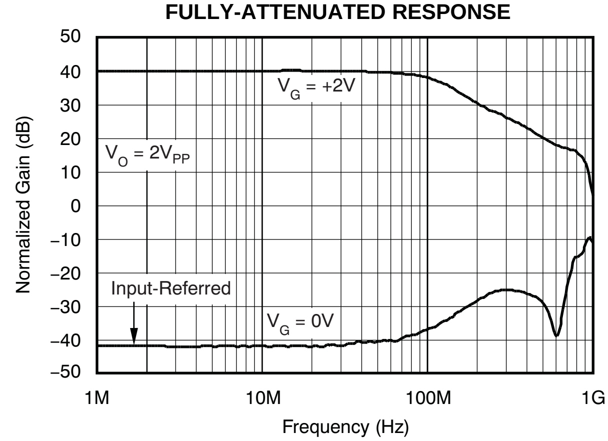


Figure 71.

INPUT LIMITED OVERDRIVE RECOVERY

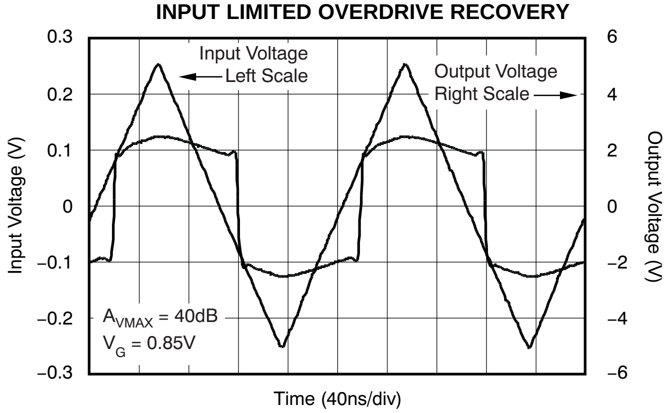


Figure 72.

OUTPUT LIMITED OVERDRIVE RECOVERY

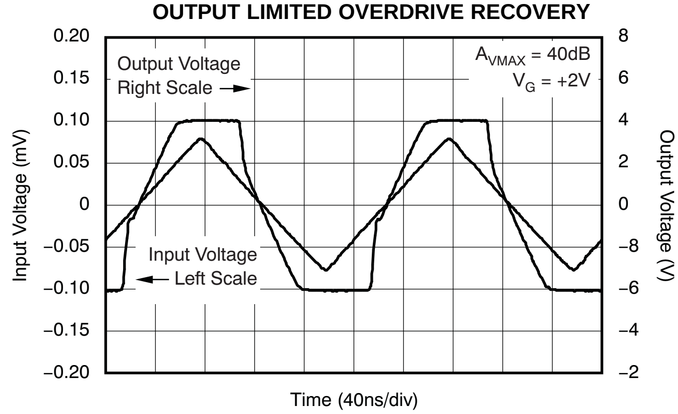


Figure 73.

TYPICAL CHARACTERISTICS: V_S = ±5V, A_{VMAX} = 40dB (continued)

At T_A = +25°C, R_L = 100Ω, R_F = 845Ω, R_G = 16.9Ω, V_G = +2V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

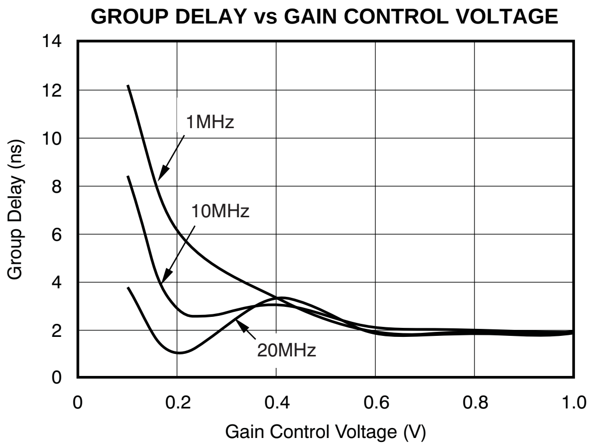


Figure 74.

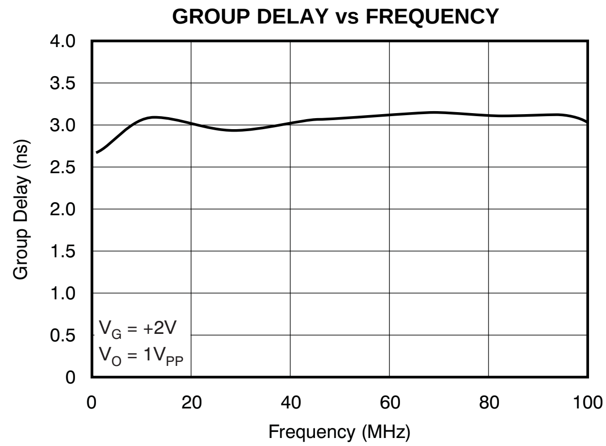


Figure 75.

APPLICATION INFORMATION

WIDEBAND VARIABLE GAIN AMPLIFIER OPERATION

The VCA820 provides an exceptional combination of high output power capability with a wideband, greater than 40dB gain adjust range, linear in dB variable gain amplifier. The VCA820 input stage places the transconductance element between two input buffers, using the output currents as the forward signal. As the differential input voltage rises, a signal current is generated through the gain element. This current is then mirrored and gained by a factor of two before reaching the multiplier. The other input of the multiplier is the voltage gain control pin, V_G. Depending on the voltage present on V_G, up to two times the gain current is provided to the transimpedance output stage. The transimpedance output stage is a current-feedback amplifier providing high output current capability and high slew rate, 1700V/µs. This exceptional full-power performance comes at the price of a relatively high quiescent current (34mA), but a low input voltage noise for this type of architecture (8.2nV/$\sqrt{Hz}$).

Figure 76 shows the dc-coupled, gain of 20dB, dual power-supply circuit used as the basis of the ±5V Electrical Characteristics and Typical Characteristics.

For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the Electrical Characteristics table are taken directly at the input and output pins, while output power (dBm) is at the matched 50Ω load. For the circuit in Figure 76, the total effective load is 100Ω ∥ 1kΩ. Note that for the SO-14 package, there is a ground pin, GND (pin 11). For the SO-14 package, this pin must be connected to ground through a 20Ω resistor in order to avoid possible oscillations of the output stage. In the MSOP-10 package, this pin is internally connected and does not require such precaution. An X2Y™ capacitor has been used for power-supply bypassing. The combination of low inductance, high resonance frequency, and integration of three capacitors in one package (two capacitors to ground and one across the supplies) of this capacitor enables to achieve the low second-harmonic distortion reported in the Electrical Characteristics table. More information on how the VCA820 operates can be found in the *Operating Suggestions* section.

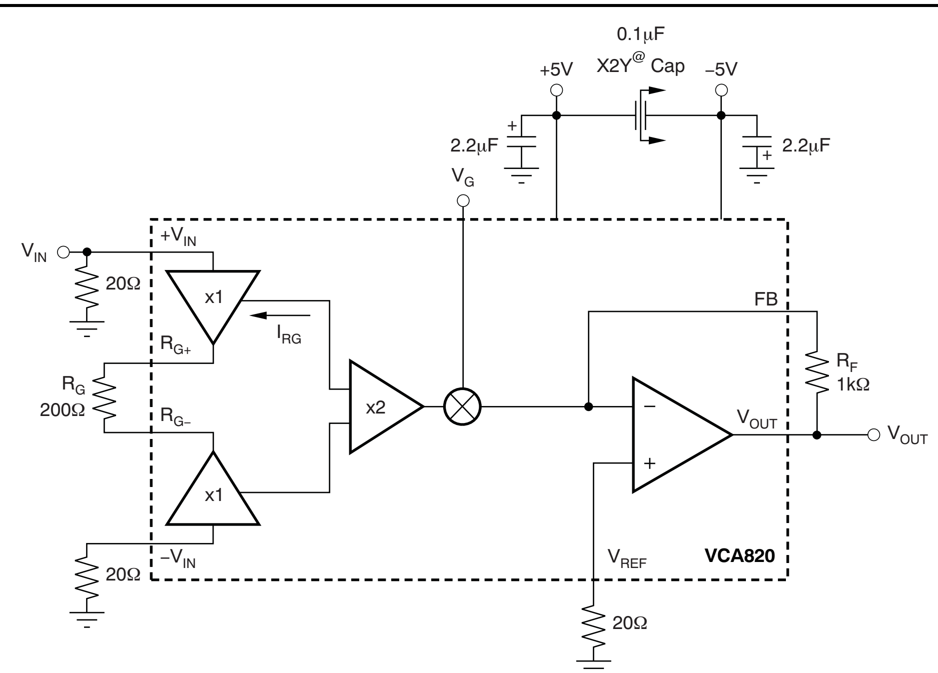


Figure 76. DC-Coupled, A_{VMAX} = 20dB, Bipolar Supply Specification and Test Circuit

DIFFERENCE AMPLIFIER

Because both inputs of the VCA820 are high-impedance, a difference amplifier can be implemented without any major problem. This implementation is shown in Figure 77. This circuit provides excellent common-mode rejection ratio (CMRR) as long as the input is within the CMRR range of –2.1V to +1.6V. Note that this circuit does not make use of the gain control pin, V_G. Also, it is recommended to choose R_S such that the pole formed by R_S and the parasitic input capacitance does not limit the bandwidth of the circuit. The common-mode rejection ratio for this circuit implemented in a gain of 20dB for V_G = +2V is shown in Figure 78. Note that because the gain control voltage is fixed and is normally set to +2V, the feedback element can be reduced in order to increase the bandwidth. When reducing the feedback element make sure that the VCA820 is not limited by common-mode input voltage, the current flowing through R_G, or any other limitation described in this data sheet.

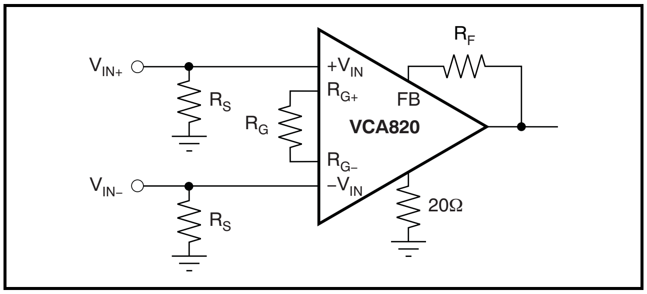


Figure 77. Difference Amplifier

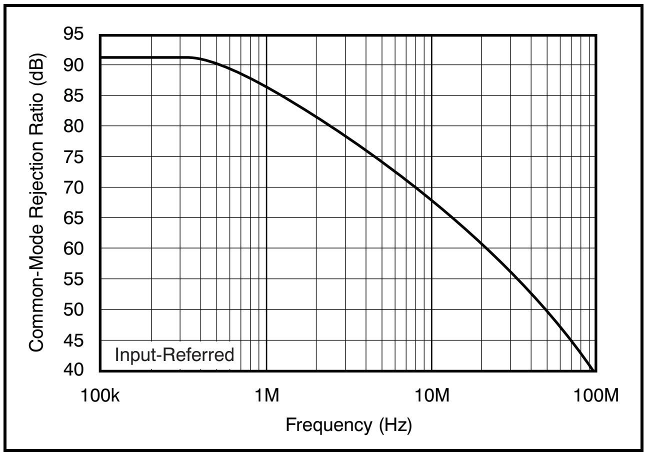


Figure 78. Common-Mode Rejection Ratio

DIFFERENTIAL EQUALIZER

If the application requires frequency shaping (the transition from one gain to another), the VCA820 can be used advantageously because its architecture allows the application to isolate the input from the gain setting elements. Figure 79 shows an implementation of such a configuration. The transfer function is shown in Equation 1.

$$G = 2 \times \frac{R_F}{R_G} \times \frac{1 + sR_GC_1}{1 + sR_1C_1} \quad (1)$$

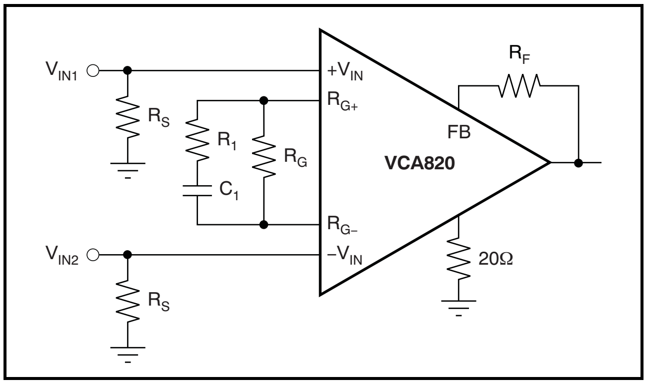


Figure 79. Differential Equalizer

This transfer function has one pole, P_1 (located at R_GC_1), and one zero, Z_1 (located at R_1C_1). When equalizing an RC load, R_L and C_L, compensate the pole added by the load located at R_LC_L with the zero Z_1. Knowing R_L, C_L, and R_G allows the user to select C_1 as a first step and then calculate R_1. Using R_L = 75Ω, C_L = 100pF and wanting the VCA820 to operate at a gain of +2V/V, which gives $R_F = R_G$ = 1.33kΩ, allows the user to select C_1 = 5pF to ensure a positive value for the resistor R_1. With all these values known, R_1 can be calculated to be 170Ω. The frequency response for both the initial, unequalized frequency response and the resulting equalized frequency response are illustrated in Figure 80.

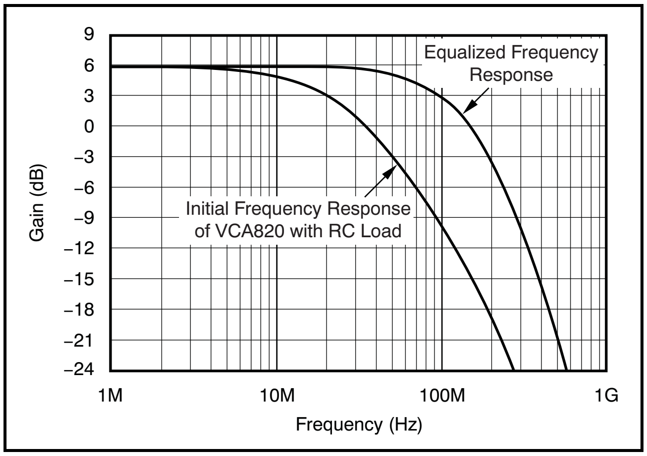


Figure 80. Differential Equalization of an RC Load

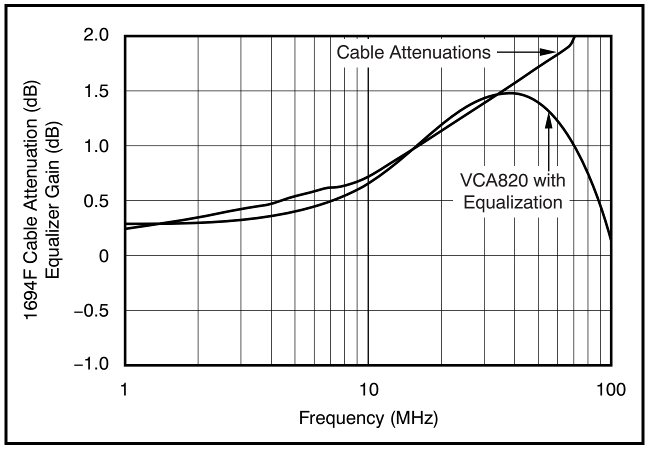


Figure 81. Cable Attenuation versus Equalizer Gain

DIFFERENTIAL CABLE EQUALIZER

A differential cable equalizer can easily be implemented using the VCA820. An example of a cable equalization for 100 feet of Belden Cable 1694F is illustrated in Figure 82, with the result for this implementation shown in Figure 81. This implementation has a maximum error of 0.2dB from dc to 40MHz.

Note that this implementation shows the cable attenuation side-by-side with the equalization in the same plot. For a given frequency, the equalization function realized with the VCA820 matches the cable attenuation. The circuit in Figure 82 is a driver circuit. To implement a receiver circuit, the signal is received differentially between the $+V_{IN}$ and $–V_{IN}$ inputs.

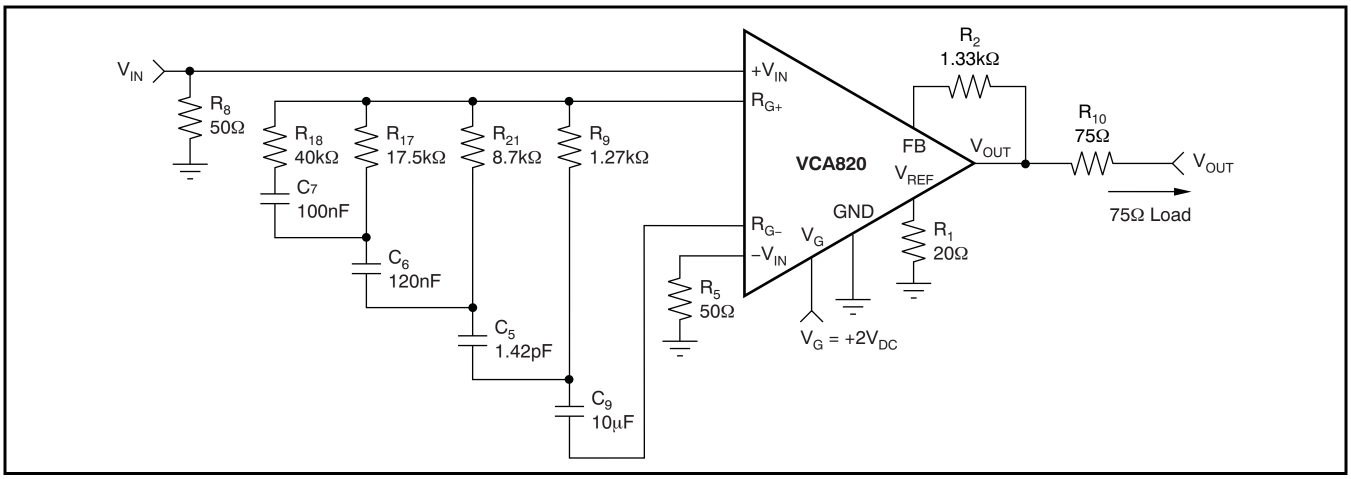


Figure 82. Differential Cable Equalizer

AGC LOOP

In the typical AGC loop shown in Figure 83, the OPA695 follows the VCA820 to provide 40dB of overall gain. The output of the OPA695 is rectified and integrated by an OPA820 to control the gain of the VCA820. When the output level exceeds the reference voltage (V_{REF}), the integrator ramps down reducing the gain of the AGC loop. Conversely, if the output is too small, the integrator ramps up increasing the net gain and the output voltage.

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the VCA820 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. EVM Ordering Information

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
VCA820ID	SO-14	DEM-VCA-SO-1B	SBOU050
VCA820IDGS	MSOP-10	DEM-VCA-MSOP-1A	SBOU051

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the VCA820 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This principle is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role in circuit performance. A SPICE model for the VCA820 is available through the TI web page. The applications group is also available for design assistance. The models available from TI predict typical small-signal ac performance, transient steps, dc performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the relevant product data sheet.

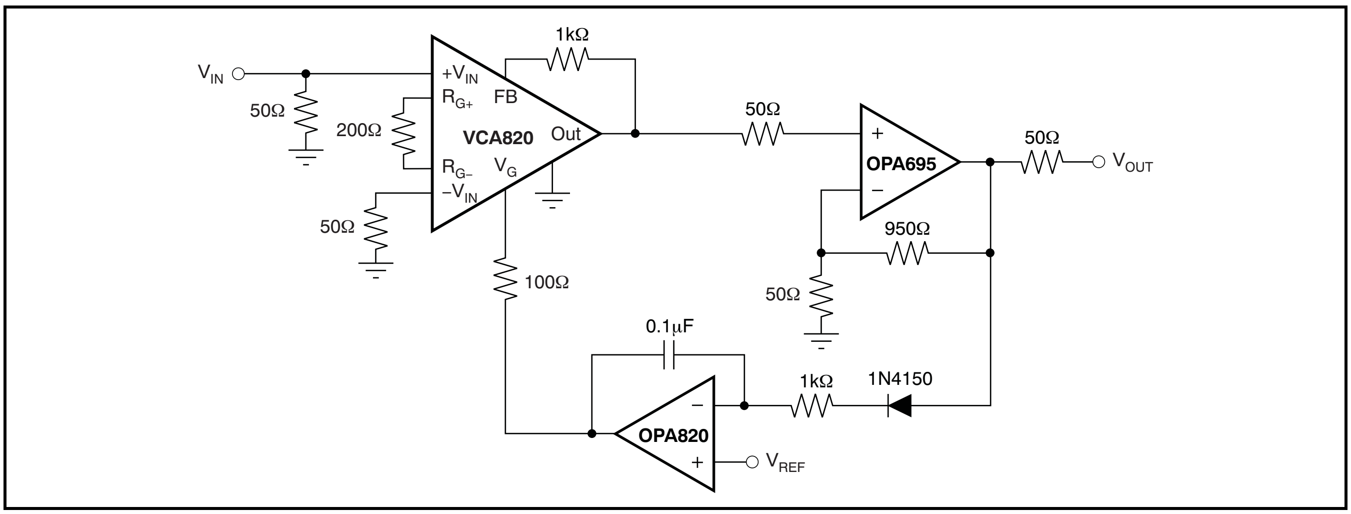


Figure 83. AGC Loop

OPERATING SUGGESTIONS

Operating the VCA820 optimally for a specific application requires trade-offs between bandwidth, input dynamic range and the maximum input voltage, the maximum gain of operation and gain, output dynamic range and the maximum input voltage, the package used, loading, and layout and bypass recommendations. The Typical Characteristics have been defined to cover as much ground as possible to describe the VCA820 operation. There are four sections in the Typical Characteristics:

- V_S = ±5V DC Parameters and V_S = ±5V DC and Power-Supply Parameters, which include dc operation and the intrinsic limitation of a VCA820 design
- V_S = ±5V, A_{VMAX} = 6dB Gain of 6dB Operation
- V_S = ±5V, A_{VMAX} = 20dB Gain of 20dB Operation
- V_S = ±5V, A_{VMAX} = 40dB Gain of 40dB Operation

Where the Typical Characteristics describe the actual performance that can be achieved by using the amplifier properly, the following sections describe in detail the trade-offs needed to achieve this level of performance.

PACKAGE CONSIDERATIONS

The VCA820 is available in both SO-14 and MSOP-10 packages. Each package has, for the different gains used in the typical characteristics, different values of R_F and R_G in order to achieve the same performance detailed in the Electrical Characteristics table.

Figure 84 shows a test gain circuit for the VCA820. Table 2 lists the recommended configuration for the SO-14 and MSOP-10 package.

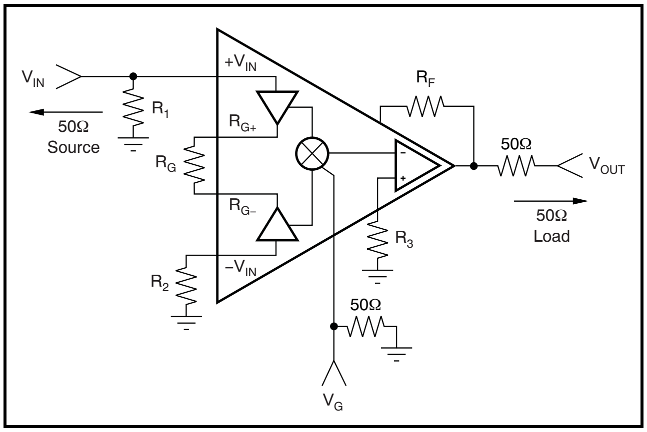


Figure 84. Test Circuit

Table 2. SO-14 and MSOP-10 R_F and R_G Configurations

	G = 2	G = 10	G = 100
R_F	1.33kΩ	1kΩ	845Ω
R_G	1.33kΩ	200Ω	16.9Ω

There are no differences between the packages in the recommended values for the gain and feedback resistors. However, the bandwidth for the VCA820IDGS (MSOP-10 package) is lower than the bandwidth for the VCA820ID (SO-14 package). This difference is true for all gains, but especially true for gains greater than 5V/V, as can be seen in Figure 85 and Figure 86. Note that the scale must be changed to a linear scale to view the details.

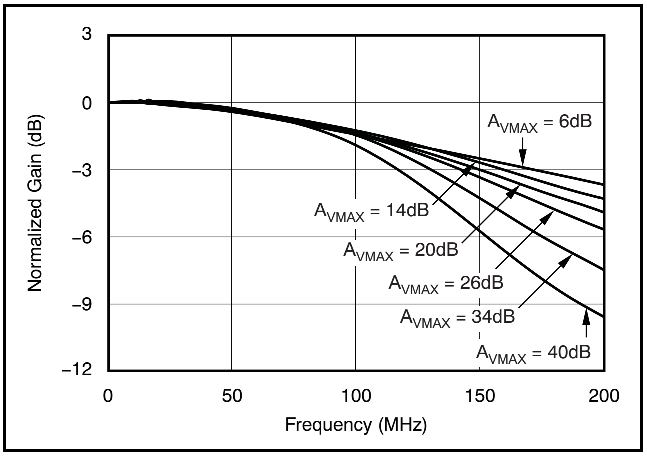


Figure 85. SO-14 Recommended R_F and R_G versus A_{VMAX}

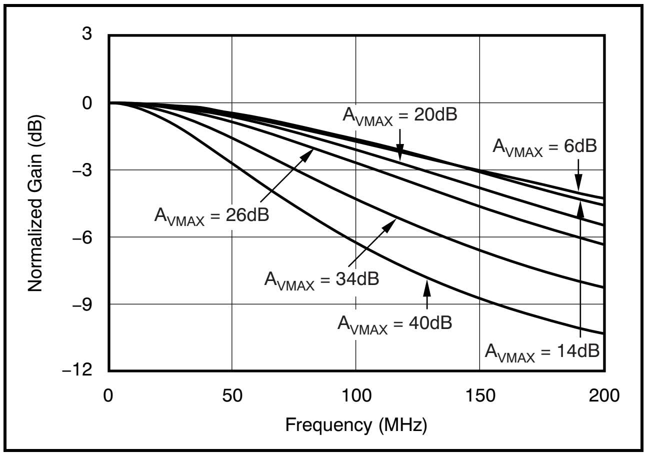


Figure 86. MSOP-10 Recommended R_F and R_G versus A_{VMAX}

MAXIMUM GAIN OF OPERATION

This section describes the use of the VCA820 in a fixed-gain application in which the V_G control pin is set at V_G = +2V. The tradeoffs described here are with bandwidth, gain, and output voltage range.

In the case of an application that does not make use of the V_{GAIN}, but requires some other characteristic of the VCA820, the R_G resistor must be set such that the maximum current flowing through the resistance I_{RG} is less than ±2.6mA typical, or $5.2mA_{PP}$ as defined in the Electrical Characteristics table, and must follow Equation 2.

$$I_{RG} = \frac{V_{OUT}}{A_{VMAX} \times R_G} \quad (2)$$

As illustrated in Equation 2, once the output dynamic range and maximum gain are defined, the gain resistor is set. This gain setting in turn affects the bandwidth, because in order to achieve the gain (and with a set gain element), the feedback element of the output stage amplifier is set as well. Keeping in mind that the output amplifier of the VCA820 is a current-feedback amplifier, the larger the feedback element, the lower the bandwidth as the feedback resistor is the compensation element.

Limiting the discussion to the input voltage only and ignoring the output voltage and gain, Figure 3 illustrates the tradeoff between the input voltage and the current flowing through the gain resistor.

OUTPUT CURRENT AND VOLTAGE

The VCA820 provides output voltage and current capabilities that are unsurpassed in a low-cost monolithic VCA. Under no-load conditions at +25°C, the output voltage typically swings closer than 1V to either supply rails; the +25°C swing limit is within 1.2V of either rails. Into a 15Ω load (the minimum tested load), it is tested to deliver more than ±160mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or *V-I product*, that is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot (Figure 50) in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the VCA820 output drive capabilities, noting that the graph is bounded by a *Safe Operating Area* of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the VCA820 can drive ±2.5V into 25Ω or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±3.9V output swing capability, as shown in the Typical Characteristics.

The minimum specified output voltage and current over-temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup do the output current and voltage decrease to the numbers shown in the Electrical Characteristics tables. As the output transistors deliver power, the respective junction temperatures increase, increasing the available output voltage swing, and increasing the available output current. In steady-state operation, the available output voltage and current is always greater than that temperature shown in the over-temperature specifications because the output stage junction temperatures are higher than the specified operating ambient.

INPUT VOLTAGE DYNAMIC RANGE

The VCA820 has a input dynamic range limited to +1.6V and –2.1V. Increasing the input voltage dynamic range can be done by using an attenuator network on the input. If the VCA820 is trying to regulate the amplitude at the output, such as in an AGC application, the input voltage dynamic range is directly proportional to Equation 3.

$$V_{IN(PP)} = R_G \times I_{RG(PP)} \quad (3)$$

As such, for unity-gain or under-attenuated conditions, the input voltage must be limited to the CMIR of ±1.6V (3.2V_{PP}) and the current (I_{RQ}) must flow through the gain resistor, ±2.6mA (5.2mA_{PP}). This configuration sets a minimum value for R_E such that the gain resistor has to be greater than Equation 4.

$$R_{GMIN} = \frac{3.2V_{PP}}{5.2mA_{PP}} = 615.4\Omega \quad (4)$$

Values lower than 615.4Ω are gain elements that result in reduced input range, as the dynamic input range is limited by the current flowing through the gain resistor R_G (I_{RG}). If the I_{RG} current is limiting the performance of the circuit, the input stage of the VCA820 goes into overdrive, resulting in limited output voltage range. Such I_{RG}-limited overdrive conditions are shown in Figure 52 for the gain of 20dB and Figure 72 for the 40dB gain.

OUTPUT VOLTAGE DYNAMIC RANGE

With its large output current capability and its wide output voltage swing of ±3.9V typical on 100Ω load, it is easy to forget other types of limitations that the VCA820 can encounter. For these limitations, careful analysis must be done to avoid input stage limitation, either voltage or I_{RG} current; also, consider the gain limitation, as the control pin V_G varies, affecting other aspects of the circuit.

BANDWIDTH

The output stage of the VCA820 is a wideband current-feedback amplifier. As such, the feedback resistance is the compensation of the last stage. Reducing the feedback element and maintaining the gain constant limits the useful range of I_{RG}, and therefore reducing the gain adjust range. For a given gain, reducing the gain element limits the maximum achievable output voltage swing.

OFFSET ADJUSTMENT

As a result of the internal architecture used on the VCA820, the output offset voltage originates from the output stage and from the input stage and multiplier core. Figure 88 illustrates how to compensate both sources of the output offset voltage. Use this procedure to compensate the output offset voltage: starting with the output stage compensation, set V_G = 0V to eliminate all offset contribution of the input stage and multiplier core. Adjust the output stage offset compensation potentiometer. Finally, set V_G = +1V to the maximum gain and adjust the input stage and multiplier core potentiometer. This procedure effectively eliminates all offset contribution at the maximum gain. Because adjusting the gain modifies the contribution of the input stage and the multiplier core, some residual output offset voltage remains.

NOISE

The VCA820 offers 8.2nV/√Hz input-referred voltage noise density at a gain of 20dB and 1.8pA/√Hz input-referred current noise density. The input-referred voltage noise density considers that all noise terms, except the input current noise but including the thermal noise of both the feedback resistor and the gain resistor, are expressed as one term.

This model is formulated in Equation 5 and Figure 87.

$$e_O = A_{VMAX} \times \sqrt{2 \times (R_S \times i_n)^2 + e_n^{\,2} + 2 \times 4kTR_S} \quad (5)$$

A more complete model is illustrated in Figure 89. For additional information on this model and the actual modeled noise terms, please contact the High-Speed Product Application Support team at www.ti.com.

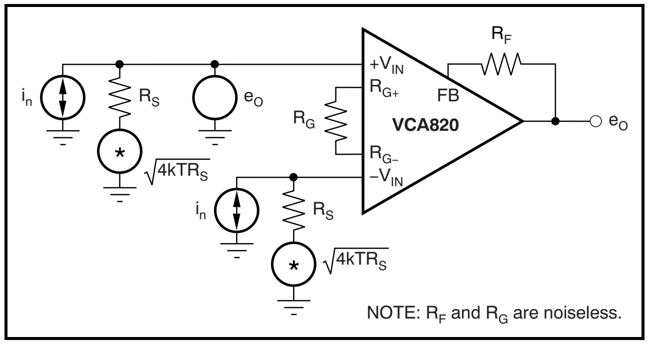


Figure 87. Simple Noise Model

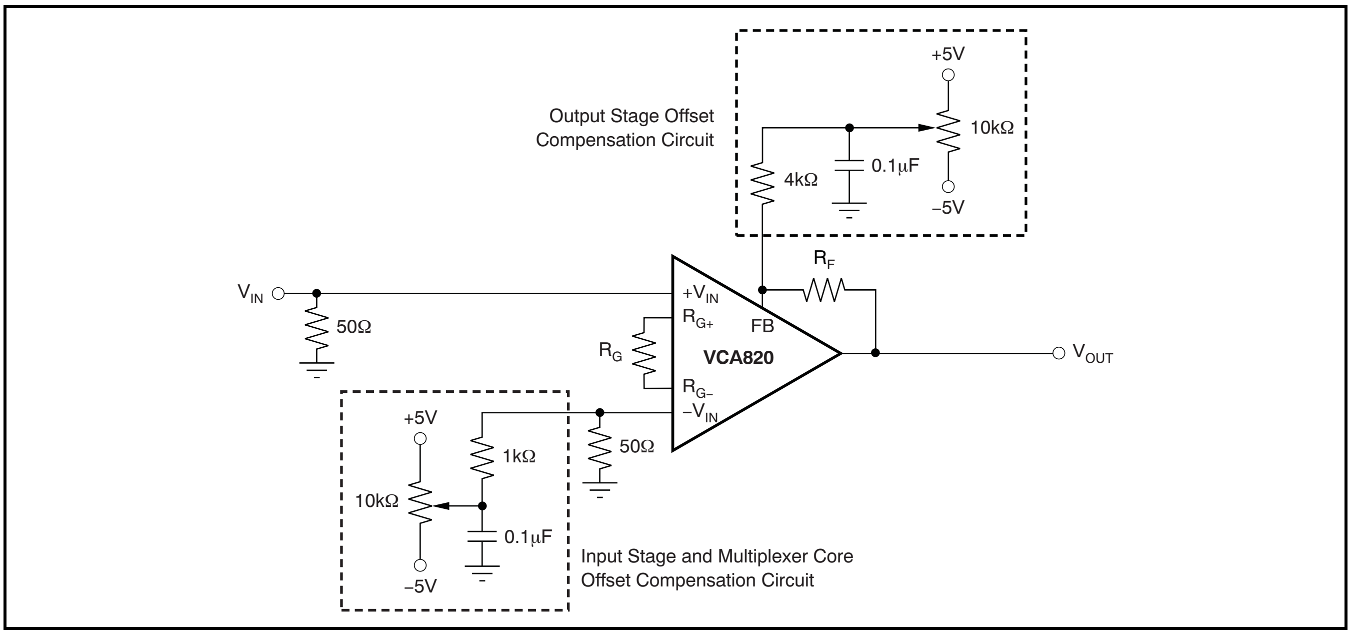


Figure 88. Adjusting the Input and Output Voltage Sources

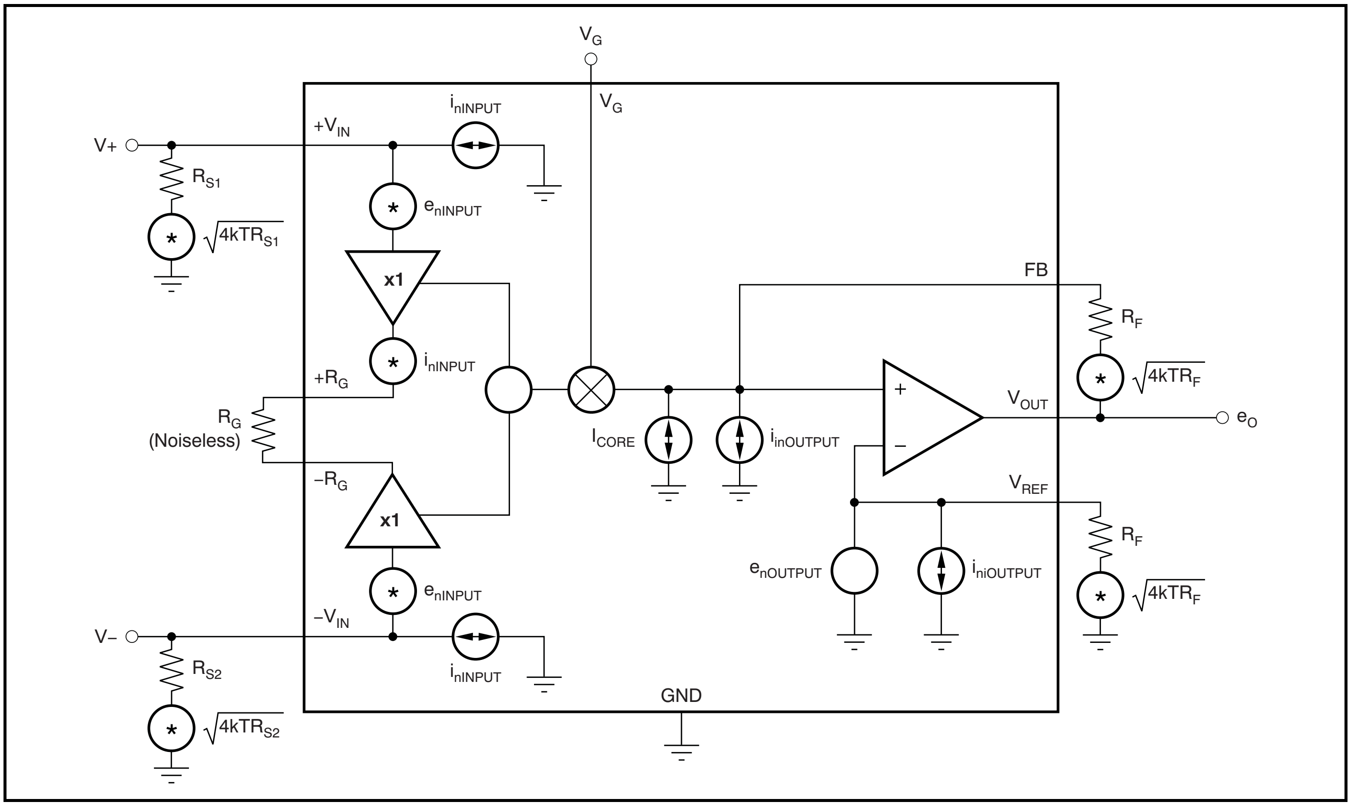


Figure 89. Full Noise Model

THERMAL ANALYSIS

The VCA820 does not require heatsinking or airflow in most applications. The maximum desired junction temperature sets the maximum allowed internal power dissipation as described in this section. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by Equation 6:

$$T_J = T_A + P_D \times \theta_{JA} \quad (6)$$

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load, however, it is at a maximum when the output is fixed at a voltage equal to one-half of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \times R_L)$, where R_L is the resistive load.

Note that it is the power in the output stage and not in the load that determines internal power dissipation. As a worst-case example, compute the maximum T_J using a VCA820ID (SO-14 package) in the circuit of Figure 76 operating at maximum gain and at the maximum specified ambient temperature of +85°C.

$$P_D = 10V(38mA) + 5^2/(4 \times 100\Omega) = 442.5mW \quad (7)$$

$$\text{Maximum } T_J = +85°C + (0.449W \times 80°C/W) = 120.5°C \quad (8)$$

This maximum operating junction temperature is well below most system level targets. Most applications should be lower because an absolute worst-case output stage power was assumed in this calculation of $V_{CC}/2$, which is beyond the output voltage range for the VCA820.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier such as the VCA820 requires careful attention to printed circuit board (PCB) layout parasitics and external component types. Recommendations to optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. This recommendation includes the ground pin (pin 2). Parasitic capacitance on the output can cause instability: on both the inverting input and the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board. Place a small series resistance (greater than 25Ω) with the input pin connected to ground to help decouple package parasitics.

b) Minimize the distance (less than 0.25”) from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserve the high-frequency performance of the VCA820. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Because the output pin is the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as inverting or non-inverting input termination resistors, should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils, or 1.27mm to 2.54mm) should be used, preferably with ground and power planes opened up around them.

e) Socketing a high-speed part like the VCA820 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the VCA820 onto the board.

INPUT AND ESD PROTECTION

The VCA820 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table.

All pins on the VCA820 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply, as shown in Figure 90. These diodes begin to conduct when the pin voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To ensure long-term reliability, however, diode current should be externally limited to 10mA whenever possible.

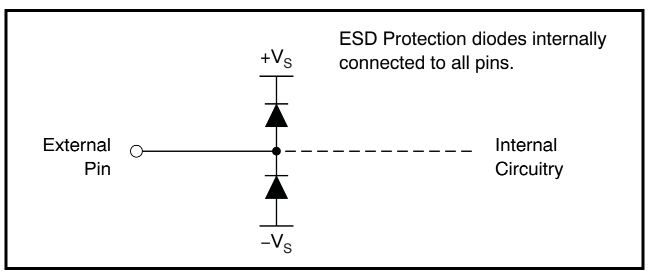


Figure 90. Internal ESD Protection

Changes from Original (October 2007) to Revision A	Page
• Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
VCA820ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
VCA820IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
VCA820IDGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
VCA820IDGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
VCA820IDGST	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
VCA820IDGSTG4	ACTIVE	MSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
VCA820IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
VCA820IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

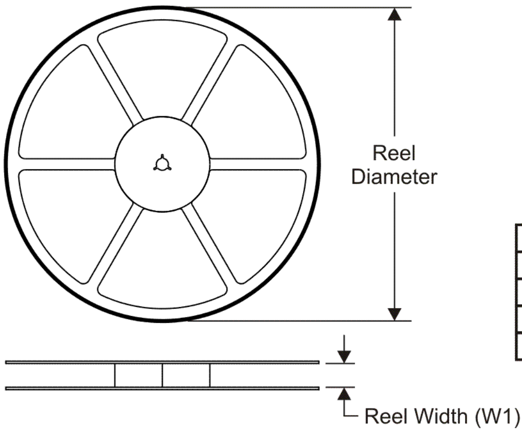
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

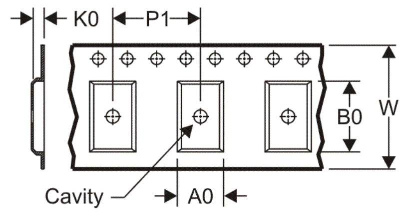
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

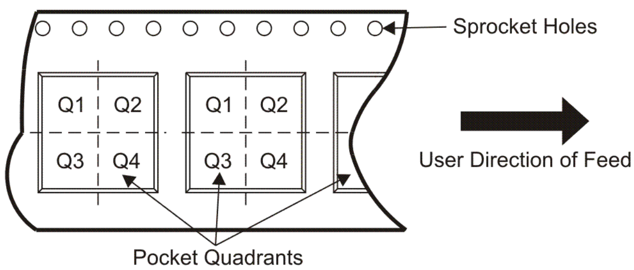


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

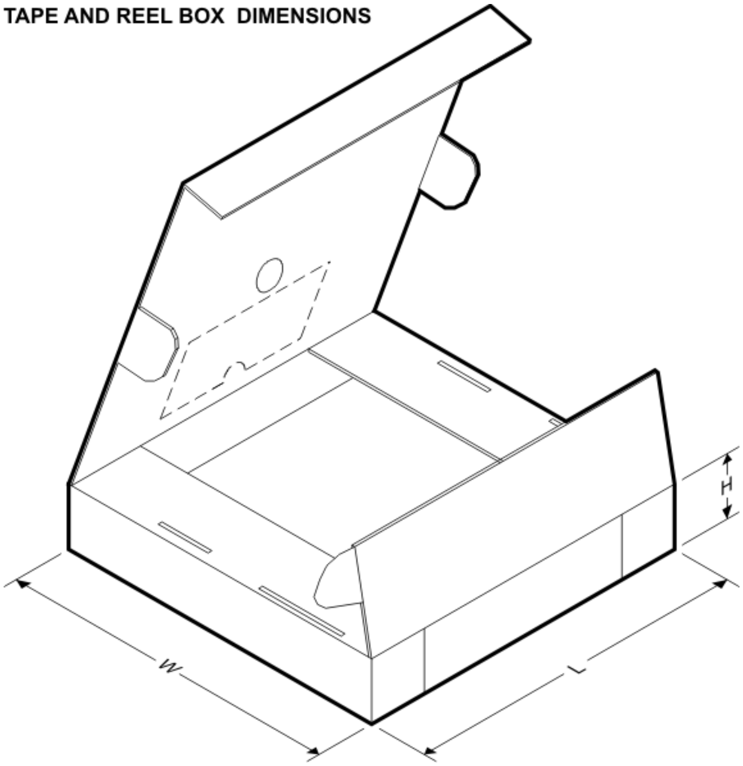
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VCA820IDGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
VCA820IDGST	MSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
VCA820IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

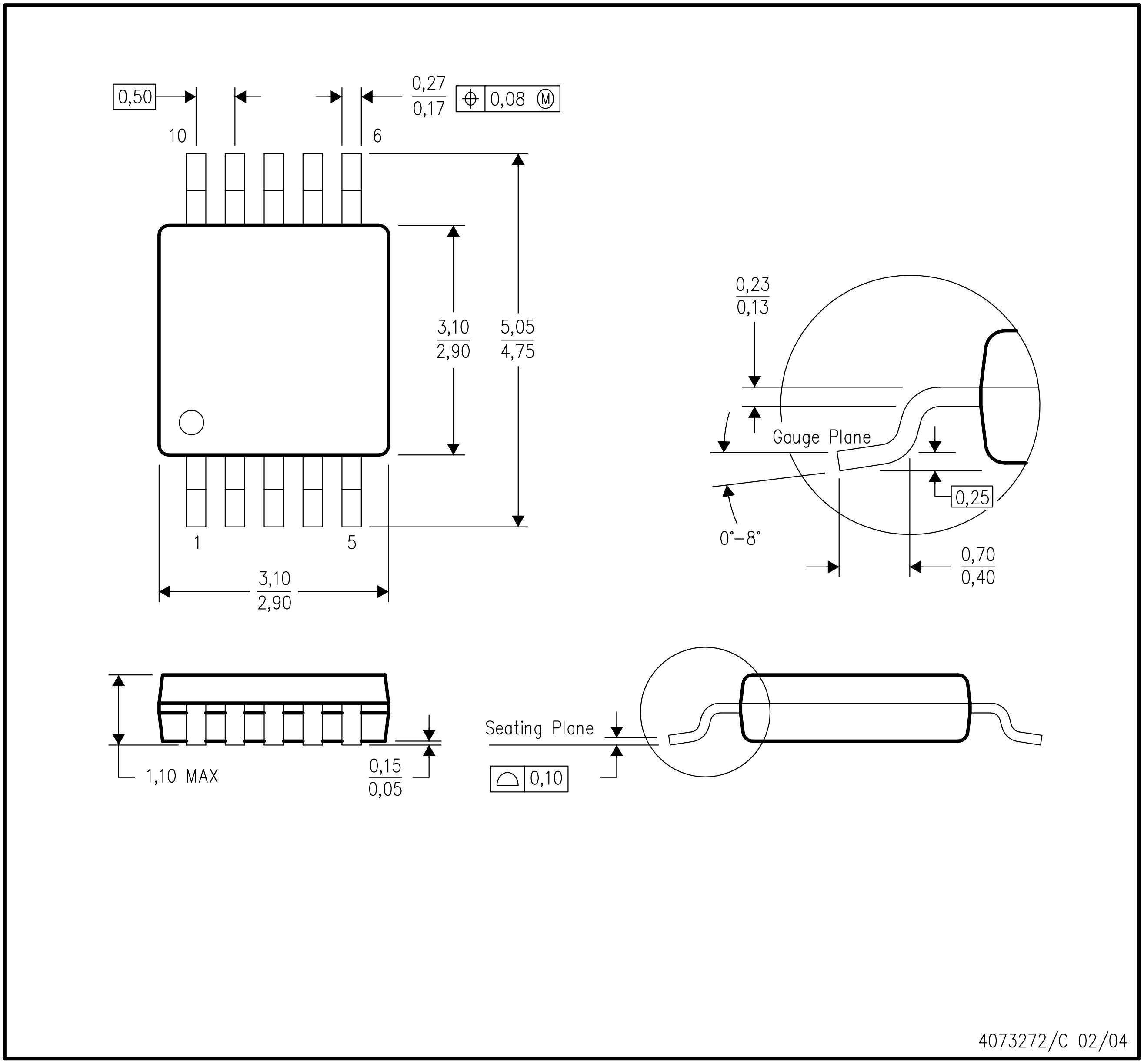
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

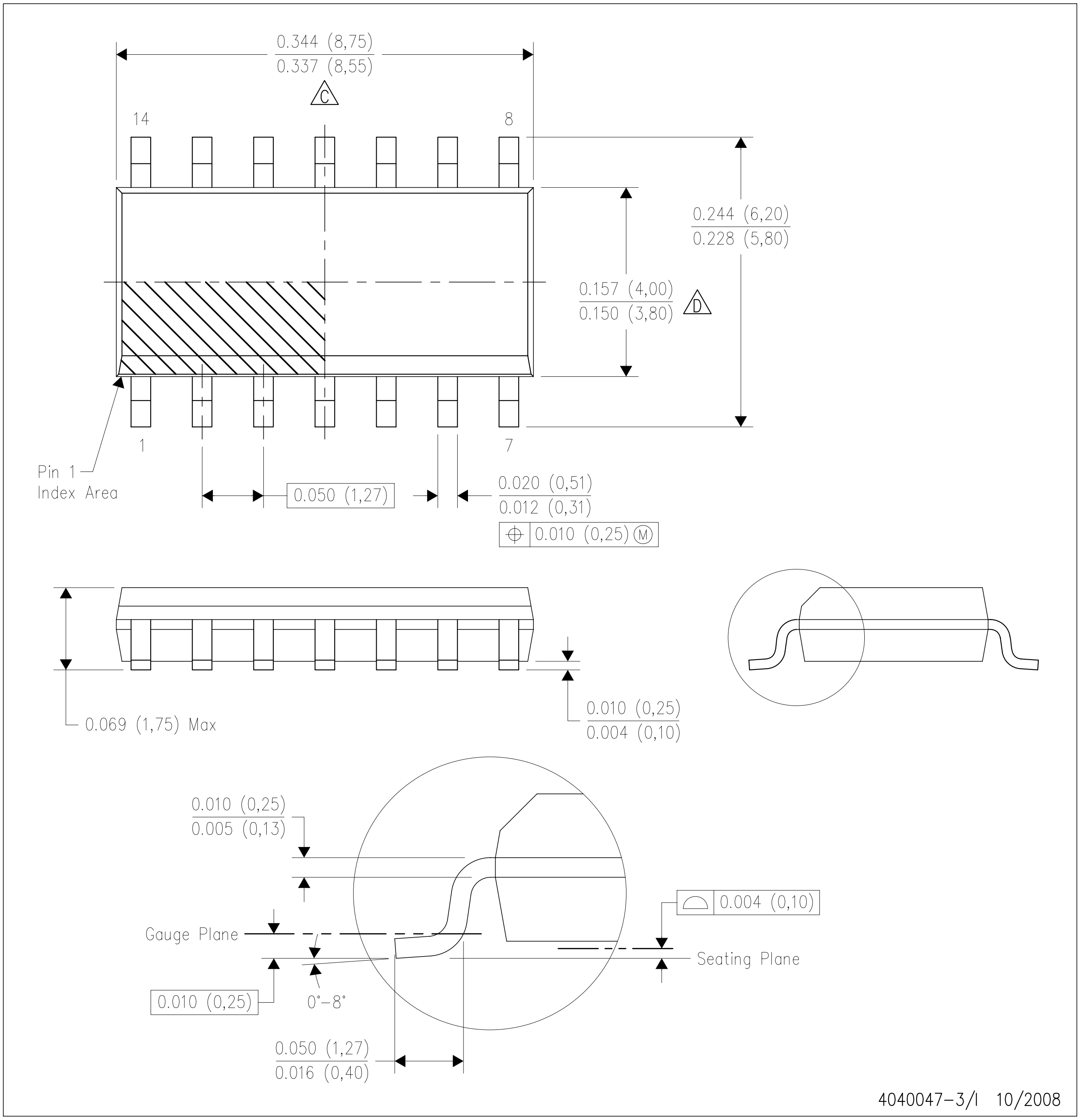
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VCA820IDGSR	MSOP	DGS	10	2500	346.0	346.0	29.0
VCA820IDGST	MSOP	DGS	10	250	190.5	212.7	31.8
VCA820IDR	SOIC	D	14	2500	346.0	346.0	33.0

DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation BA.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS–012 variation AB.